

EVLYS LTD. - POWER SEMICONDUCTORS DEVICES - Wholesale and Retail.

Fast Thyristor Type **FDT80-2000-25**

Low switching losses / Low reverse recovery charge
Distributed amplified gate for high di_T/dt

Mean on-state current	I_{TAV}		2000 A	
Repetitive peak off-state voltage	V_{DRM}		2000...2500 V	
Repetitive peak reverse voltage	V_{RRM}			
Turn-off time	t_q		40.0, 50.0, 63.0 μs	
V_{DRM}, V_{RRM}, V	2000	2200	2400	2500
Voltage code	20	22	24	25
$T_j, ^\circ C$	-60...+125			

MAXIMUM ALLOWABLE RATINGS

Symbols and parameters		Units	Values	Test conditions	
ON-STATE					
I_{TAV}	Maximum allowable mean on-state current	A	2000 2970	$T_c=85^\circ C$; Double side cooled; $T_c=55^\circ C$; Double side cooled; 180° half-sine wave; 50 Hz	
I_{TRMS}	RMS on-state current	A	3140	$T_c=85^\circ C$; Double side cooled; 180° half-sine wave; 50 Hz	
I_{TSM}	Surge on-state current	kA	45.0 52.0	$T_j=T_{jmax}$ $T_j=25^\circ C$	180° half-sine wave; $t_p=10$ ms; single pulse; $V_D=V_R=0$ V; Gate pulse: $I_G=I_{FGM}$; $V_G=20$ V; $t_{GP}=50$ μs ; $di_G/dt=2$ A/ μs
			47.0 54.0	$T_j=T_{jmax}$ $T_j=25^\circ C$	180° half-sine wave; $t_p=8.3$ ms; single pulse; $V_D=V_R=0$ V; Gate pulse: $I_G=I_{FGM}$; $V_G=20$ V; $t_{GP}=50$ μs ; $di_G/dt=2$ A/ μs
I^2t	Safety factor	$A^2s \cdot 10^3$	10100 13500	$T_j=T_{jmax}$ $T_j=25^\circ C$	180° half-sine wave; $t_p=10$ ms; single pulse; $V_D=V_R=0$ V; Gate pulse: $I_G=I_{FGM}$; $V_G=20$ V; $t_{GP}=50$ μs ; $di_G/dt=2$ A/ μs
			9100 12100	$T_j=T_{jmax}$ $T_j=25^\circ C$	180° half-sine wave; $t_p=8.3$ ms; single pulse; $V_D=V_R=0$ V; Gate pulse: $I_G=I_{FGM}$; $V_G=20$ V; $t_{GP}=50$ μs ; $di_G/dt=2$ A/ μs
BLOCKING					
V_{DRM}, V_{RRM}	Repetitive peak off-state and Repetitive peak reverse voltages	V	2000...2500	$T_{jmin} < T_j < T_{jmax}$; 180° half-sine wave; 50 Hz; Gate open	
V_{DSM}, V_{RSM}	Non-repetitive peak off-state and Non-repetitive peak reverse voltages	V	2100...2600	$T_{jmin} < T_j < T_{jmax}$; 180° half-sine wave; single pulse; Gate open	
V_D, V_R	Direct off-state and Direct reverse voltages	V	$0.6 \cdot V_{DRM}$ $0.6 \cdot V_{RRM}$	$T_j=T_{jmax}$; Gate open	

EVLYS LTD. - POWER SEMICONDUCTORS DEVICES - Wholesale and Retail.

TRIGGERING				
I_{FGM}	Peak forward gate current	A	10	$T_j = T_{j\max}$
V_{RGM}	Peak reverse gate voltage	V	5	
P_G	Gate power dissipation	W	8	$T_j = T_{j\max}$ for DC gate current
SWITCHING				
$(di_T/dt)_{crit}$	Critical rate of rise of on-state current non-repetitive (f=1 Hz)	A/ μ s	2500	$T_j = T_{j\max}$; $V_D = 0.67 \cdot V_{DRM}$; $I_{TM} = 8000$ A; Gate pulse: $I_G = 2$ A; $V_G = 20$ V; $t_{GP} = 50$ μ s; $di_G/dt = 2$ A/ μ s
THERMAL				
T_{stg}	Storage temperature	$^{\circ}$ C	-60...+50	
T_j	Operating junction temperature	$^{\circ}$ C	-60...+125	
MECHANICAL				
F	Mounting force	kN	40.0...50.0	
a	Acceleration	m/s ²	50	Device clamped

CHARACTERISTICS

Symbols and parameters		Units	Values	Conditions	
ON-STATE					
V_{TM}	Peak on-state voltage, max	V	2.15	$T_j = 25$ $^{\circ}$ C; $I_{TM} = 6280$ A	
$V_{T(TO)}$	On-state threshold voltage, max	V	1.265	$T_j = T_{j\max}$;	
r_T	On-state slope resistance, max	m Ω	0.150	$0.5 \pi I_{TAV} < I_T < 1.5 \pi I_{TAV}$	
I_H	Holding current, max	mA	1000	$T_j = 25$ $^{\circ}$ C; $V_D = 12$ V; Gate open	
BLOCKING					
I_{DRM}, I_{RRM}	Repetitive peak off-state and Repetitive peak reverse currents, max	mA	300	$T_j = T_{j\max}$; $V_D = V_{DRM}$; $V_R = V_{RMIN}$	
$(dv_D/dt)_{crit}$	Critical rate of rise of off-state voltage ¹⁾ , min	V/ μ s	200, 320, 500, 1000, 1600, 2000, 2500	$T_j = T_{j\max}$; $V_D = 0.67 \cdot V_{DRM}$; Gate open	
TRIGGERING					
V_{GT}	Gate trigger direct voltage, max	V	3.00 3.00 1.50	$T_j = T_{j\min}$ $T_j = 25$ $^{\circ}$ C $T_j = T_{j\max}$	$V_D = 12$ V; $I_D = 3$ A; Direct gate current
I_{GT}	Gate trigger direct current, max	mA	500 300 150	$T_j = T_{j\min}$ $T_j = 25$ $^{\circ}$ C $T_j = T_{j\max}$	
V_{GD}	Gate non-trigger direct voltage, min	V	0.35	$T_j = T_{j\max}$; $V_D = 0.67 \cdot V_{DRM}$;	
I_{GD}	Gate non-trigger direct current, min	mA	70.00	Direct gate current	
SWITCHING					
t_{gd}	Delay time, max	μ s	1.10	$T_j = 25$ $^{\circ}$ C; $V_D = 1000$ V; $I_{TM} = I_{TAV}$; $di/dt = 200$ A/ μ s;	
t_{gt}	Turn-on time ²⁾ , max	μ s	2.50, 3.20, 4.00, 6.30	Gate pulse: $I_G = 2$ A; $V_G = 20$ V; $t_{GP} = 50$ μ s; $di_G/dt = 2$ A/ μ s	
t_q	Turn-off time ³⁾ , max	μ s	40.0, 50.0, 63.0 50.0, 63.0, 80.0	$dv_D/dt = 50$ V/ μ s; $dv_D/dt = 200$ V/ μ s;	$T_j = T_{j\max}$; $I_{TM} = I_{TAV}$; $di_R/dt = -10$ A/ μ s; $V_R = 100$ V; $V_D = 0.67 V_{DRM}$
Q_{rr}	Recovered charge, max	μ C	1250	$T_j = T_{j\max}$; $I_{TM} = 1000$ A;	
t_{rr}	Reverse recovery time, max	μ s	10	$di_R/dt = -50$ A/ μ s;	
I_{rr}	Reverse recovery current, max	A	250	$V_R = 100$ V	

EVLYS LTD. - POWER SEMICONDUCTORS DEVICES - Wholesale and Retail.

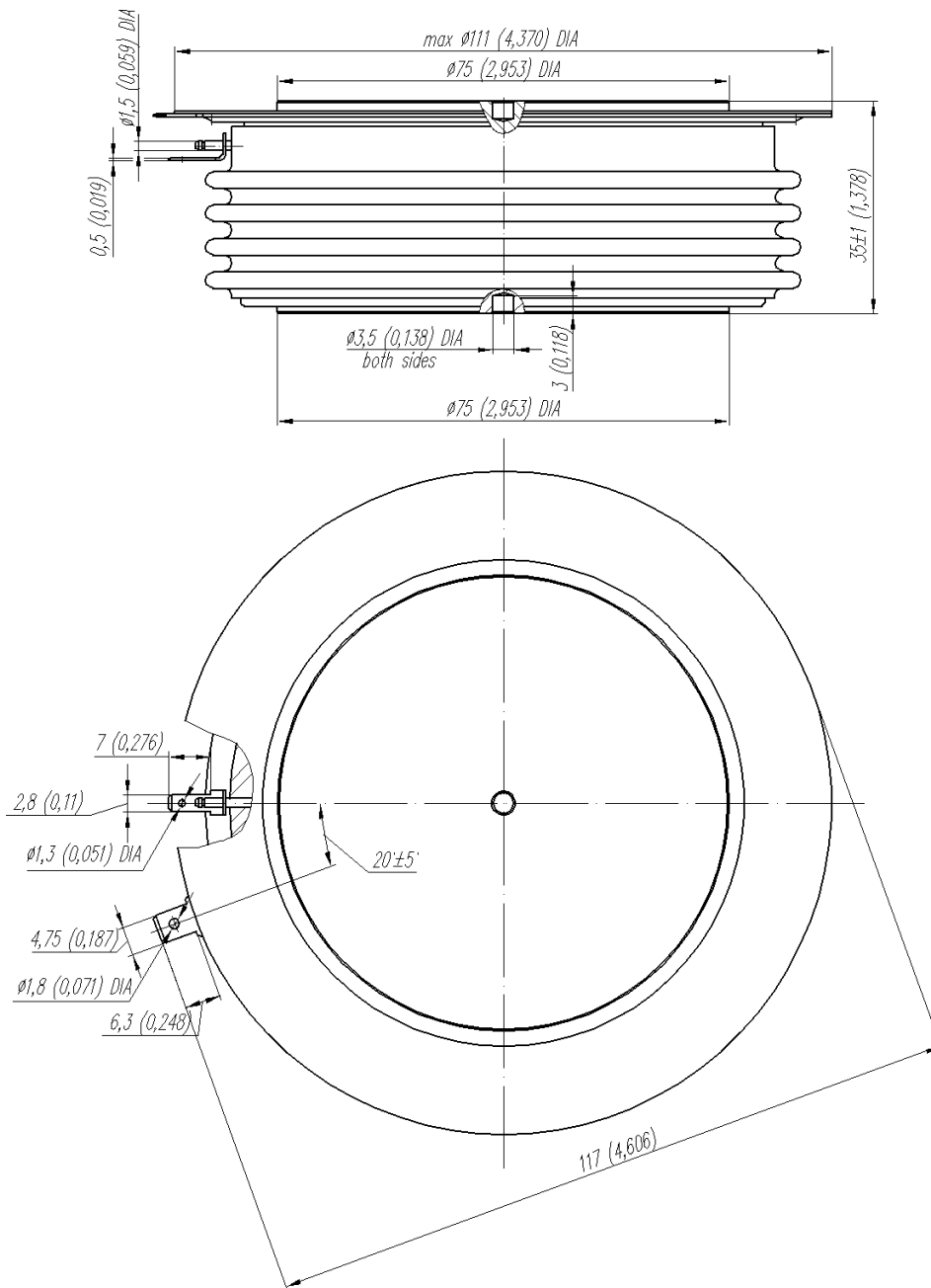
THERMAL					
R_{thjc}	Thermal resistance, junction to case, max	°C/W	0.0100	Direct current	Double side cooled
R_{thjc-A}			0.0220		Anode side cooled
R_{thjc-K}			0.0180		Cathode side cooled
R_{thck}	Thermal resistance, case to heatsink, max	°C/W	0.0020	Direct current	
MECHANICAL					
m	Weight, max	g	1600		
D_s	Surface creepage distance	mm (inch)	55.13 (2.170)		
D_a	Air strike distance	mm (inch)	25.10 (0.988)		

PART NUMBERING GUIDE								NOTES																							
FDT	80	2000	25	7	2	3		¹⁾ Critical rate of rise of off-state voltage																							
1	2	3	4	5	6	7		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Symbol of Group</th> <th>4</th> <th>5</th> <th>6</th> <th>7</th> <th>8</th> <th>8,5</th> <th>9</th> </tr> </thead> <tbody> <tr> <td>$(dv_D/dt)_{crit}, V/\mu s$</td> <td>200</td> <td>320</td> <td>500</td> <td>1000</td> <td>1600</td> <td>2000</td> <td>2500</td> </tr> </tbody> </table>								Symbol of Group	4	5	6	7	8	8,5	9	$(dv_D/dt)_{crit}, V/\mu s$	200	320	500	1000	1600	2000	2500
Symbol of Group	4	5	6	7	8	8,5	9																								
$(dv_D/dt)_{crit}, V/\mu s$	200	320	500	1000	1600	2000	2500																								
1. FDT — Fast Inverter Disc Thyristor 2. Design version 3. Mean on-state current, A 4. Voltage code 5. Critical rate of rise of off-state voltage 6. Group of turn-off time ($dv_D/dt=50 V/\mu s$) 7. Group of turn-on time								²⁾ Turn-on time																							
								<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Symbol of group</th> <th>4</th> <th>3</th> <th>2</th> <th></th> </tr> </thead> <tbody> <tr> <td>$t_{gt}, \mu s$</td> <td>2.50</td> <td>3.20</td> <td>4.00</td> <td>6.30</td> </tr> </tbody> </table>								Symbol of group	4	3	2		$t_{gt}, \mu s$	2.50	3.20	4.00	6.30						
Symbol of group	4	3	2																												
$t_{gt}, \mu s$	2.50	3.20	4.00	6.30																											
								³⁾ Turn-off time ($dv_D/dt=50 V/\mu s$)																							
								<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Symbol of group</th> <th>3</th> <th>2</th> <th>1</th> </tr> </thead> <tbody> <tr> <td>$t_q, \mu s$</td> <td>40.0</td> <td>50.0</td> <td>63.0</td> </tr> </tbody> </table>								Symbol of group	3	2	1	$t_q, \mu s$	40.0	50.0	63.0								
Symbol of group	3	2	1																												
$t_q, \mu s$	40.0	50.0	63.0																												

EVLYS LTD. - POWER SEMICONDUCTORS DEVICES - Wholesale and Retail.

OVERALL DIMENSIONS

Package type: **T.F5**



All dimensions in millimeters (inches)