EVLYS LTD. - POWER SEMICONDUCTORS DEVICES - Wholesale and Retail.

Fast Thyristor Type FDT40-400-22

Low switching losses / Low reverse recovery charge

Distributed amplified gate for high di_T/dt

Mean on-state current		I_{TAV}	400 A
Repetitive peak off-state voltage		V_{DRM}	2000...2200 V
Repetitive peak reverse voltage		V_{RRM}	
Turn-off time		t_q	25.0, 32.0, 40.0, 50.0 μs
V_{DRM}, V_{RRM}, V	2000		2200
Voltage code	20		22
T_j, °C	–60...+125		

MAXIMUM ALLOWABLE RATINGS

Symbols and parameters		Units	Values	Test conditions	
ON-STATE					
I_{TAV}	Mean on-state current	A	400 457 677	T_c= 91 °C; Double side cooled; T_c= 85 °C; Double side cooled; T_c= 55 °C; Double side cooled; 180° half-sine wave; 50 Hz	
I_{TRMS}	RMS on-state current	A	628	T_c= 91 °C; Double side cooled; 180° half-sine wave; 50 Hz	
I_{TSM}	Surge on-state current	kA	9.0 10.5	T_j=$T_{j\,max}$ T_j=25 °C	180° half-sine wave; t_p=10 ms; single pulse; V_D=V_R=0 V; Gate pulse:I_G=I_{FGM}; V_G=20 V; t_{GP}=50 μs; di_G/dt=1 A/μs
			9.5 11.0	T_j=$T_{j\,max}$ T_j=25 °C	180° half-sine wave; t_p=8.3 ms; single pulse; V_D=V_R=0 V; Gate pulse:I_G=I_{FGM}; V_G=20 V; t_{GP}=50 μs; di_G/dt=1 A/μs
I^2t	Safety factor	$A^2s\cdot10^3$	400 550	T_j=$T_{j\,max}$ T_j=25 °C	180° half-sine wave; t_p=10 ms; single pulse; V_D=V_R=0 V; Gate pulse:I_G=I_{FGM}; V_G=20 V; t_{GP}=50 μs; di_G/dt=1 A/μs
			370 500	T_j=$T_{j\,max}$ T_j=25 °C	180° half-sine wave; t_p=8.3 ms; single pulse; V_D=V_R=0 V; Gate pulse:I_G=I_{FGM}; V_G=20 V; t_{GP}=50 μs; di_G/dt=1 A/μs
BLOCKING					
V_{DRM}, V_{RRM}	Repetitive peak off-state and Repetitive peak reverse voltages	V	2000...2200	$T_{j\,min}$< T_j <$T_{j\,max}$; 180° half-sine wave; 50 Hz; Gate open	
V_{DSM}, V_{RSM}	Non-repetitive peak off-state and Non-repetitive peak reverse voltages	V	2100...2300	$T_{j\,min}$< T_j <$T_{j\,max}$; 180° half-sine wave; single pulse; Gate open	
V_D, V_R	Direct off-state and Direct reverse voltages	V	0.6·V_{DRM} 0.6·V_{RRM}	T_j=$T_{j\,max}$; Gate open	

TRIGGERING				
I_{FGM}	Peak forward gate current	A	8	$T_j=T_{j\,max}$
V_{RGM}	Peak reverse gate voltage	V	5	
P_G	Gate power dissipation	W	8	$T_j=T_{j\,max}$ for DC gate current
SWITCHING				
$(di_T/dt)_{crit}$	Critical rate of rise of on-state current non-repetitive (f=1 Hz)	A/µs	2000	$T_j=T_{j\,max}$; $V_D=0.67\cdot V_{DRM}$; $I_{TM}=2500$ A; Gate pulse: $I_G=2$ A; $V_G=20$ V; $t_{GP}=50$ µs; $di_G/dt=2$ A/µs
THERMAL				
T_{stg}	Storage temperature	°C	–60...+50	
T_j	Operating junction temperature	°C	–60...+125	
MECHANICAL				
F	Mounting force	kN	14.0...16.0	
a	Acceleration	m/s^2	50	Device clamped

CHARACTERISTICS

Symbols and parameters		Units	Values	Conditions	
ON-STATE					
V_{TM}	Peak on-state voltage, max	V	2.85	$T_j=25$ °C; $I_{TM}=1256$ A	
$V_{T(TO)}$	On-state threshold voltage, max	V	1.821	$T_j=T_{j\,max}$; $0.5\,\pi\,I_{TAV} < I_T < 1.5\,\pi\,I_{TAV}$	
r_T	On-state slope resistance, max	mΩ	0.976		
I_H	Holding current, max	mA	500	$T_j=25$ °C; $V_D=12$ V; Gate open	
BLOCKING					
I_{DRM}, I_{RRM}	Repetitive peak off-state and Repetitive peak reverse currents, max	mA	100	$T_j=T_{j\,max}$; $V_D=V_{DRM}$; $V_R=V_{RRM}$	
$(dv_D/dt)_{crit}$	Critical rate of rise of off-state voltage[1], min	V/µs	200, 320, 500, 1000, 1600, 2000, 2500	$T_j=T_{j\,max}$; $V_D=0.67\cdot V_{DRM}$; Gate open	
TRIGGERING					
V_{GT}	Gate trigger direct voltage, max	V	3.00 2.50 1.50	$T_j=T_{j\,min}$ $T_j=25$ °C $T_j=T_{j\,max}$	$V_D=12$ V; $I_D=3$ A; Direct gate current
I_{GT}	Gate trigger direct current, max	mA	500 300 150	$T_j=T_{j\,min}$ $T_j=25$ °C $T_j=T_{j\,max}$	
V_{GD}	Gate non-trigger direct voltage, min	V	0.35	$T_j=T_{j\,max}$; $V_D=0.67\cdot V_{DRM}$; Direct gate current	
I_{GD}	Gate non-trigger direct current, min	mA	55.00		
SWITCHING					
t_{gd}	Delay time, max	µs	0.90	$T_j=25$ °C; $V_D=1000$ V; $I_{TM}=I_{TAV}$; $di/dt=200$ A/µs; Gate pulse: $I_G=2$ A; $V_G=20$ V; $t_{GP}=50$ µs; $di_G/dt=2$ A/µs	
t_{gt}	Turn-on time[2], max	µs	1.60, 2.00, 2.50, 3.20		
t_q	Turn-off time[3] max	µs	25.0, 32.0, 40.0, 50.0	$dv_D/dt=50$ V/µs;	$T_j=T_{j\,max}$; $I_{TM}=I_{TAV}$; $di_R/dt=-10$ A/µs; $V_R=100$V; $V_D=0.67\cdot V_{DRM}$
			32.0, 40.0, 50.0, 63.0	$dv_D/dt=200$ V/µs;	
Q_{rr}	Total recovered charge, max	µC	300	$T_j=T_{j\,max}$; $I_{TM}=I_{TAV}$; $di_R/dt=-50$ A/µs; $V_R=100$ V	
t_{rr}	Reverse recovery time, typ	µs	5.0		
I_{rrM}	Peak reverse recovery current, max	A	145		

THERMAL					
R_{thjc}	Thermal resistance, junction to case, max	°C/W	0.0300	Direct current	Double side cooled
R_{thjc-A}			0.0660		Anode side cooled
R_{thjc-K}			0.0540		Cathode side cooled
R_{thck}	Thermal resistance, case to heatsink, max	°C/W	0.0060	Direct current	
MECHANICAL					
w	Weight, max	g	180		
D_s	Surface creepage distance	mm (inch)	7.86 (0.309)		
D_a	Air strike distance	mm (inch)	6.10 (0.240)		

PART NUMBERING GUIDE

FDT	40	400	22	7	5	4
1	2	3	4	5	6	7

1. FDT — Fast Inverter Disc Thyristor
2. Design version
3. Mean on-state current, A
4. Voltage code
5. Critical rate of rise of off-state voltage
6. Group of turn-off time (dv_D/dt=50 V/μs)
7. Group of turn-on time

NOTES

[1] Critical rate of rise of off-state voltage

Symbol of Group	4	5	6	7	8	8,5	9
$(dv_D/dt)_{crit}$, V/μs	200	320	500	1000	1600	2000	2500

[2] Turn-on time

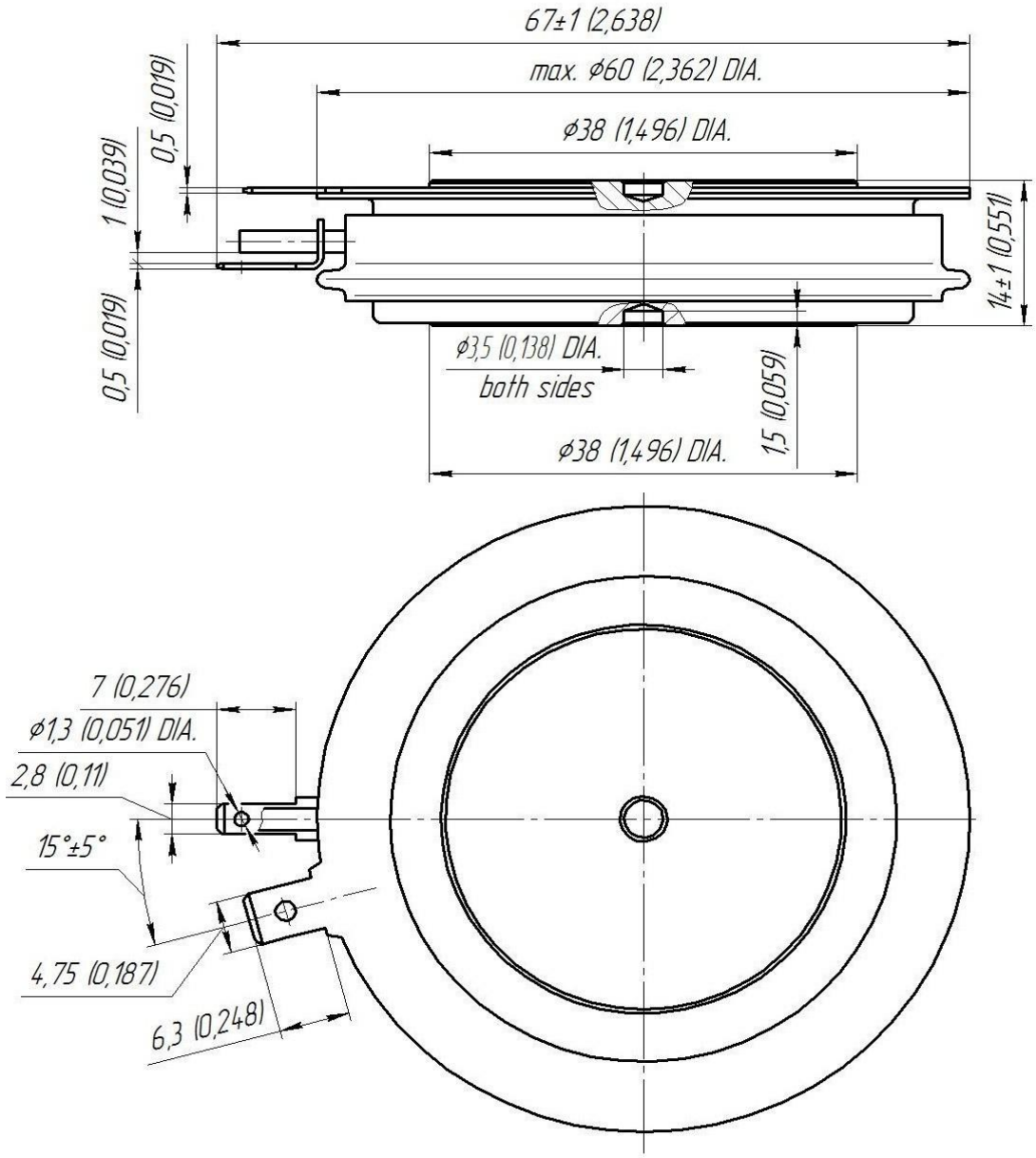
Symbol of group	6	5	4	3
t_{gt}, μs	1.60	2.00	2.50	3.20

[3] Turn-off time (dv_D/dt=50 V/μs)

Symbol of group	5	4	3	2
t_q, μs	25.0	32.0	40.0	50.0

OVERALL DIMENSIONS

Package type: T.C1



All dimensions in millimeters (inches)