

EVLYS LTD. - POWER SEMICONDUCTORS DEVICES - Wholesale and Retail.

Fast Thyristor Type FDT32-400-12

Low switching losses / Low reverse recovery charge
Distributed amplified gate for high di_T/dt

Mean on-state current		I_{TAV}	400 A
Repetitive peak off-state voltage		V_{DRM}	1000...1200 V
Repetitive peak reverse voltage		V_{RRM}	
Turn-off time		t_q	10.0, 12.5, 16.0, 20.0 μs
V_{DRM}, V_{RRM}, V	1000	1100	1200
Voltage code	10	11	12
$T_j, ^\circ C$	-60...+125		

MAXIMUM ALLOWABLE RATINGS

Symbols and parameters		Units	Values	Test conditions
ON-STATE				
I_{TAV}	Mean on-state current	A	400 435 645	$T_c = 89^\circ C$; Double side cooled; $T_c = 85^\circ C$; Double side cooled; $T_c = 55^\circ C$; Double side cooled; 180° half-sine wave; 50 Hz
I_{TRMS}	RMS on-state current	A	628	$T_c = 89^\circ C$; Double side cooled; 180° half-sine wave; 50 Hz
I_{TSM}	Surge on-state current	kA	7.0 8.0	$T_j = T_{jmax}$ $T_j = 25^\circ C$ 180° half-sine wave; $t_p = 10$ ms; single pulse; $V_D = V_R = 0$ V; Gate pulse: $I_G = I_{FGM}$; $V_G = 20$ V; $t_{GP} = 50$ μs ; $di_G/dt = 1$ A/ μs
			7.5 8.5	$T_j = T_{jmax}$ $T_j = 25^\circ C$ 180° half-sine wave; $t_p = 8.3$ ms; single pulse; $V_D = V_R = 0$ V; Gate pulse: $I_G = I_{FGM}$; $V_G = 20$ V; $t_{GP} = 50$ μs ; $di_G/dt = 1$ A/ μs
I^2t	Safety factor	$A^2s \cdot 10^3$	240 320	$T_j = T_{jmax}$ $T_j = 25^\circ C$ 180° half-sine wave; $t_p = 10$ ms; single pulse; $V_D = V_R = 0$ V; Gate pulse: $I_G = I_{FGM}$; $V_G = 20$ V; $t_{GP} = 50$ μs ; $di_G/dt = 1$ A/ μs
			230 290	$T_j = T_{jmax}$ $T_j = 25^\circ C$ 180° half-sine wave; $t_p = 8.3$ ms; single pulse; $V_D = V_R = 0$ V; Gate pulse: $I_G = I_{FGM}$; $V_G = 20$ V; $t_{GP} = 50$ μs ; $di_G/dt = 1$ A/ μs
BLOCKING				
V_{DRM}, V_{RRM}	Repetitive peak off-state and Repetitive peak reverse voltages	V	1000...1200	$T_{jmin} < T_j < T_{jmax}$; 180° half-sine wave; 50 Hz; Gate open
V_{DSM}, V_{RSM}	Non-repetitive peak off-state and Non-repetitive peak reverse voltages	V	1100...1300	$T_{jmin} < T_j < T_{jmax}$; 180° half-sine wave; single pulse; Gate open
V_D, V_R	Direct off-state and Direct reverse voltages	V	$0.6 \cdot V_{DRM}$ $0.6 \cdot V_{RRM}$	$T_j = T_{jmax}$; Gate open

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TRIGGERING				
I_{FGM}	Peak forward gate current	A	6	$T_j = T_{j\max}$
V_{RGM}	Peak reverse gate voltage	V	5	
P_G	Gate power dissipation	W	3	$T_j = T_{j\max}$ for DC gate current
SWITCHING				
$(di_T/dt)_{crit}$	Critical rate of rise of on-state current non-repetitive (f=1 Hz)	A/ μ s	1600	$T_j = T_{j\max}$; $V_D = 0.67 \cdot V_{DRM}$; $I_{TM} = 1100$ A; Gate pulse: $I_G = I_{FGM}$; $V_G = 20$ V; $t_{GP} = 50$ μ s; $di_G/dt = 2$ A/ μ s
THERMAL				
T_{stg}	Storage temperature	$^{\circ}$ C	-60...+50	
T_j	Operating junction temperature	$^{\circ}$ C	-60...+125	
MECHANICAL				
F	Mounting force	kN	9.0...11.0	
a	Acceleration	m/s ²	50	Device clamped

CHARACTERISTICS

Symbols and parameters		Units	Values	Conditions	
ON-STATE					
V_{TM}	Peak on-state voltage, max	V	2.40	$T_j = 25$ $^{\circ}$ C; $I_{TM} = 1256$ A	
$V_{T(TO)}$	On-state threshold voltage, max	V	1.430	$T_j = T_{j\max}$;	
r_T	On-state slope resistance, max	m Ω	0.812	$0.5 \pi I_{TAV} < I_T < 1.5 \pi I_{TAV}$	
I_H	Holding current, max	mA	500	$T_j = 25$ $^{\circ}$ C; $V_D = 12$ V; Gate open	
BLOCKING					
I_{DRM}, I_{RRM}	Repetitive peak off-state and Repetitive peak reverse currents, max	mA	50	$T_j = T_{j\max}$; $V_D = V_{DRM}$; $V_R = V_{RRM}$	
$(dv_D/dt)_{crit}$	Critical rate of rise of off-state voltage ¹⁾ , min	V/ μ s	200, 320, 500, 1000, 1600, 2000, 2500	$T_j = T_{j\max}$; $V_D = 0.67 \cdot V_{DRM}$; Gate open	
TRIGGERING					
V_{GT}	Gate trigger direct voltage, max	V	3.00 2.50 1.50	$T_j = T_{j\min}$ $T_j = 25$ $^{\circ}$ C $T_j = T_{j\max}$	$V_D = 12$ V; $I_D = 3$ A; Direct gate current
I_{GT}	Gate trigger direct current, max	mA	500 300 150	$T_j = T_{j\min}$ $T_j = 25$ $^{\circ}$ C $T_j = T_{j\max}$	
V_{GD}	Gate non-trigger direct voltage, min	V	0.40	$T_j = T_{j\max}$; $V_D = 0.67 \cdot V_{DRM}$;	
I_{GD}	Gate non-trigger direct current, min	mA	40.00	Direct gate current	
SWITCHING					
t_{gd}	Delay time, max	μ s	0.60	$T_j = 25$ $^{\circ}$ C; $V_D = 600$ V; $I_{TM} = I_{TAV}$; $di/dt = 200$ A/ μ s;	
t_{gt}	Turn-on time ²⁾ , max	μ s	1.25, 1.60, 2.00, 2.50	Gate pulse: $I_G = I_{FGM}$; $V_G = 20$ V; $t_{GP} = 50$ μ s; $di_G/dt = 2$ A/ μ s	
t_q	Turn-off time ³⁾ max	μ s	10.0, 12.5, 16.0, 20.0	$dv_D/dt = 50$ V/ μ s	$T_j = T_{j\max}$; $I_{TM} = 400$ A; $di_R/dt = -10$ A/ μ s; $V_R = 100$ V; $V_D = 0.67 V_{DRM}$
			12.5, 16.0, 20.0, 25.0	$dv_D/dt = 200$ V/ μ s	
Q_{rr}	Total recovered charge, max	μ C	100	$T_j = T_{j\max}$; $I_{TM} = 400$ A;	
t_{rr}	Reverse recovery time, typ	μ s	3.2	$di_R/dt = -50$ A/ μ s;	
I_{rrM}	Peak reverse recovery current, max	A	80	$V_R = 100$ V	

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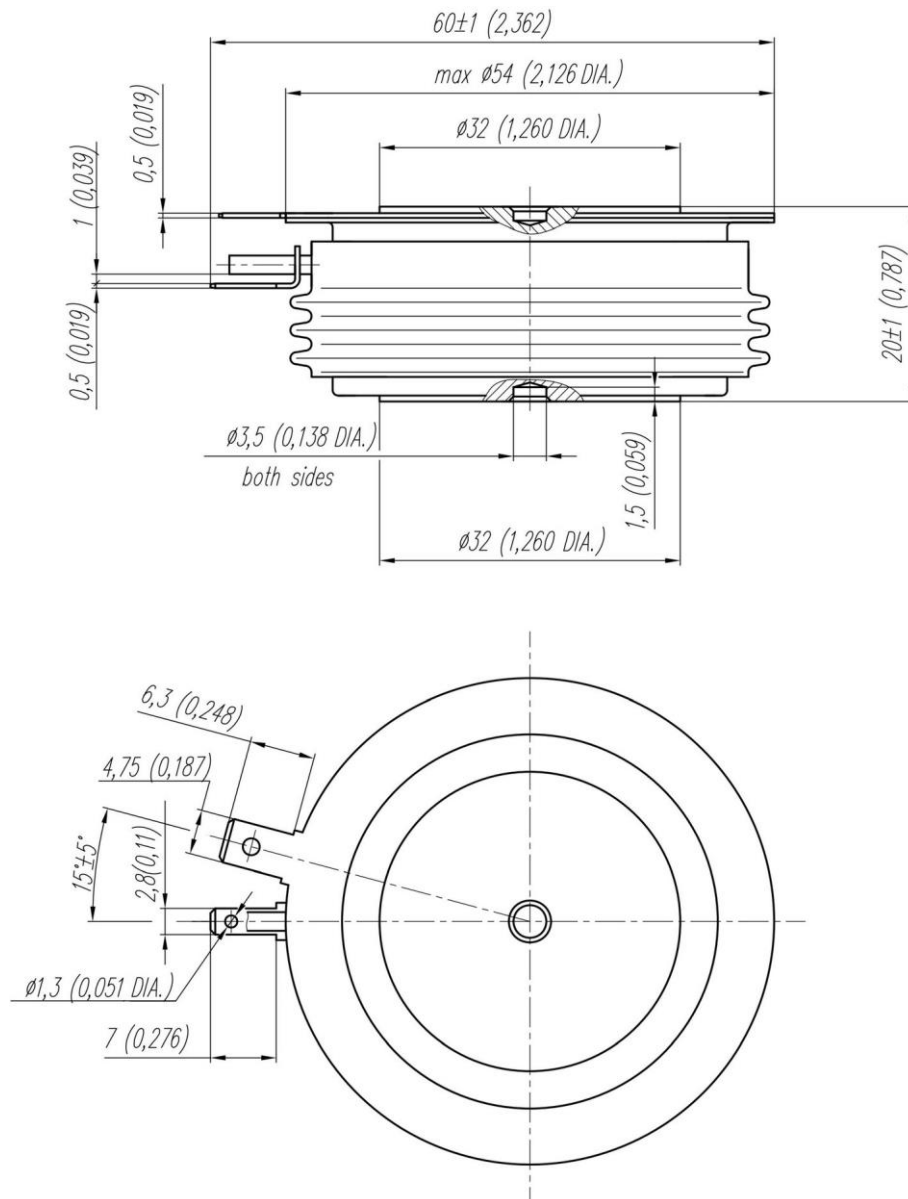
THERMAL					
R _{thjc}	Thermal resistance, junction to case, max	°C/W	0.0400	Direct current	Double side cooled
R _{thjc-A}			0.0880		Anode side cooled
R _{thjc-K}			0.0720		Cathode side cooled
R _{thck}	Thermal resistance, case to heatsink, max	°C/W	0.0060	Direct current	
MECHANICAL					
w	Weight, max	g	176		
D _s	Surface creepage distance	mm (inch)	19.44 (0.765)		
D _a	Air strike distance	mm (inch)	12.10 (0.476)		

PART NUMBERING GUIDE								NOTES									
TFI	433	400	12	A2	P3	M4	N	Symbol of Group	P2	K2	E2	A2	T1	P1	M1		
1	2	3	4	5	6	7	8	1) $(dv/dt)_{crit}$, V/ μ s	200	320	500	1000	1600	2000	2500		
1. TFI — fast inverter thyristor 2. Design version 3. Mean on-state current, A 4. Voltage code 5. Critical rate of rise of off-state voltage 6. Group of turn-off time ($dv_D/dt=50$ V/ μ s) 7. Group of turn-on time 8. Ambient conditions: N – normal; T – tropical								Symbol of group	X4	T4	P4	M4					
								2) Turn-on time	1.25	1.60	2.00	2.50					
								Symbol of group	A4	X3	T3	P3					
								3) Turn-off time ($dv_D/dt=50$ V/ μ s)	10.0	13.5	16.0	20.0					

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OVERALL DIMENSIONS

Package type: T.B3



All dimensions in millimeters (inches)

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