EVLYS LTD. - POWER SEMICONDUCTORS DEVICES - Wholesale and Retail.

Phase Control Disc Thyristor Type DT99-3600-36

High power cycling capability / Low on-state and switching losses
Designed for traction and industrial applications

Mean on-state current	I_{TAV}	3600 A			
Repetitive peak off-state voltage	V_{DRM}	3000...3600 V			
Repetitive peak reverse voltage	V_{RRM}				
Turn-off time	t_q	630 μs			
V_{DRM}, V_{RRM}, V	3000	3200	3400	3600	
Voltage code	30	32	34	36	
T_j, °C	−60...+125				

MAXIMUM ALLOWABLE RATINGS

Symbols and parameters		Units	Values	Test conditions	
ON-STATE					
I_{TAV}	Maximum allowable mean on-state current	A	3600 4930	T_c= 91 °C, Double side cooled T_c= 70 °C, Double side cooled 180° half-sine wave; 50 Hz	
I_{TRMS}	RMS on-state current	A	5652	T_c= 91 °C, Double side cooled 180° half-sine wave; 50 Hz	
I_{TSM}	Surge on-state current	kA	72.0 83.0	T_j=$T_{j\,max}$ T_j=25 °C	180° half-sine wave; t_p=10 ms; single pulse; V_D=V_R=0 V; Gate pulse: I_G=2 A; t_{GP}=50 μs; di_G/dt≥1 A/μs
			76.0 87.0	T_j=$T_{j\,max}$ T_j=25 °C	180° half-sine wave; t_p=8.3 ms; single pulse; V_D=V_R=0 V; Gate pulse: I_G=2 A; t_{GP}=50 μs; di_G/dt≥1 A/μs
I^2t	Safety factor	$A^2s·10^3$	25900 34400	T_j=$T_{j\,max}$ T_j=25 °C	180° half-sine wave; t_p=10 ms; single pulse; V_D=V_R=0 V; Gate pulse: I_G=2 A; t_{GP}=50 μs; di_G/dt≥1 A/μs
			23900 31400	T_j=$T_{j\,max}$ T_j=25 °C	180° half-sine wave; t_p=8.3 ms; single pulse; V_D=V_R=0 V; Gate pulse: I_G=2 A; t_{GP}=50 μs; di_G/dt≥1 A/μs
BLOCKING					
V_{DRM}, V_{RRM}	Repetitive peak off-state and Repetitive peak reverse voltages	V	3000...3600	$T_{j\,min}$< T_j <$T_{j\,max}$; 180° half-sine wave; 50 Hz; Gate open	
V_{DSM}, V_{RSM}	Non-repetitive peak off-state and Non-repetitive peak reverse voltages	V	3100...3700	$T_{j\,min}$< T_j <$T_{j\,max}$; 180° half-sine wave; single pulse; Gate open	
V_D, V_R	Direct off-state and Direct reverse voltages	V	0.6·V_{DRM} 0.6·V_{RRM}	T_j=$T_{j\,max}$; Gate open	

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TRIGGERING				
I_{FGM}	Peak forward gate current	A	12	$T_j=T_{j\,max}$
V_{RGM}	Peak reverse gate voltage	V	5	
P_G	Gate power dissipation	W	5	$T_j=T_{j\,max}$ for DC gate current
SWITCHING				
$(di_T/dt)_{crit}$	Critical rate of rise of on-state current non-repetitive (f=1 Hz)	A/μs	1000	$T_j=T_{j\,max}$; $V_D=0.67 \cdot V_{DRM}$; $I_{TM}=7200$ A; Gate pulse: $I_G=2$ A; $t_{GP}=50$ μs; $di_G/dt \geq 2$ A/μs
THERMAL				
T_{stg}	Storage temperature	°C	−60...+50	
T_j	Operating junction temperature	°C	−60...+125	
MECHANICAL				
F	Mounting force	kN	70.0...90.0	
a	Acceleration	m/s^2	50	Device clamped

CHARACTERISTICS

Symbols and parameters		Units	Values	Conditions
ON-STATE				
V_{TM}	Peak on-state voltage, max	V	1.70	$T_j=25$ °C; $I_{TM}=6300$ A
$V_{T(TO)}$	On-state threshold voltage, max	V	0.90	$T_j=T_{j\,max}$;
r_T	On-state slope resistance, max	mΩ	0.110	$0.5\,\pi\,I_{TAV} < I_T < 1.5\,\pi\,I_{TAV}$
I_L	Latching current, max	mA	1500	$T_j=25$ °C; $V_D=12$ V; Gate pulse: $I_G=2$ A; $t_{GP}=50$ μs; $di_G/dt \geq 1$ A/μs
I_H	Holding current, max	mA	300	$T_j=25$ °C; $V_D=12$ V; Gate open
BLOCKING				
I_{DRM}, I_{RRM}	Repetitive peak off-state and Repetitive peak reverse currents, max	mA	300	$T_j=T_{j\,max}$; $V_D=V_{DRM}$; $V_R=V_{RRM}$
$(dv_D/dt)_{crit}$	Critical rate of rise of off-state voltage[1], min	V/μs	500, 1000, 1600	$T_j=T_{j\,max}$; $V_D=0.67 \cdot V_{DRM}$; Gate open
TRIGGERING				
V_{GT}	Gate trigger direct voltage, max	V	5.00 / 3.00 / 2.00	$T_j= T_{j\,min}$ / $T_j=25$ °C / $T_j= T_{j\,max}$ — $V_D=12$ V; $I_D=3$ A; Direct gate current
I_{GT}	Gate trigger direct current, max	mA	500 / 300 / 200	$T_j= T_{j\,min}$ / $T_j= 25$ °C / $T_j= T_{j\,max}$
V_{GD}	Gate non-trigger direct voltage, min	V	0.35	$T_j=T_{j\,max}$; $V_D=0.67 \cdot V_{DRM}$; Direct gate current
I_{GD}	Gate non-trigger direct current, min	mA	15.00	
SWITCHING				
t_{gd}	Delay time, max	μs	3.00	$T_j=25$ °C; $V_D=1500$ V; $I_{TM}=I_{TAV}$; Gate pulse: $I_G=2$ A; $t_{GP}=50$ μs; $di_G/dt \geq 2$ A/μs
t_q	Turn-off time[2], max	μs	630	$dv_D/dt=50$ V/μs; $T_j=T_{j\,max}$; $I_{TM}=1000$ A; $di_R/dt=-10$ A/μs; $V_R=100$ V; $V_D=0.67\,V_{DRM}$
Q_{rr}	Recovered charge, max	μC	7000	$T_j=T_{j\,max}$; $I_{TM}=1000$ A; $di_R/dt=-5$ A/μs; $V_R=100$ V
t_{rr}	Reverse recovery time, max	μs	68	
I_{rr}	Reverse recovery current, max	A	205	

THERMAL					
R_{thjc}	Thermal resistance, junction to case, max	°C/W	0.0050	Direct current	Double side cooled
R_{thjc-A}			0.0110		Anode side cooled
R_{thjc-K}			0.0090		Cathode side cooled
R_{thck}	Thermal resistance, case to heatsink, max	°C/W	0.0010	Direct current	

MECHANICAL				
m	Weight, max	g	2200	
D_s	Surface creepage distance	mm (inch)	44.60 (1.756)	
D_a	Air strike distance	mm (inch)	15.70 (0.618)	

PART NUMBERING GUIDE

DT	99	3600	36	7	3
1	2	3	4	5	6

1. DT - Phase Control Disc Thyristor
2. Element Diameter
3. Mean on-state current, A
4. Voltage code
5. Critical rate of rise of on-state current non-repetitive, V/μs
6. Turn-off time (dv_D/dt=50 V/μs)

NOTES

1) Critical rate of rise of off-state voltage

Symbol of Group	6	7	8
$(dv_D/dt)_{crit}$, V/μs	500	1000	1600

2) Turn-off time (dv_D/dt=50 V/μs)

Symbol of Group	0
t_q, μs	630

OVERALL DIMENSIONS

Package type: T.G5

max ø150 (5,905) DIA

ø100 (3,937) DIA

ø1,5 (0,059) DIA

0,5 (0,019)

26±2 (1,024)

ø3,5 (0,138) DIA
both sides

3 (0,118)

ø100 (3,937) DIA

7 (0,276)

2,8 (0,11)

ø1,3 (0,051) DIA

20±5°

6,3 (0,248)

ø1,8 (0,071) DIA

4,75 (0,187)

157 (6,181)
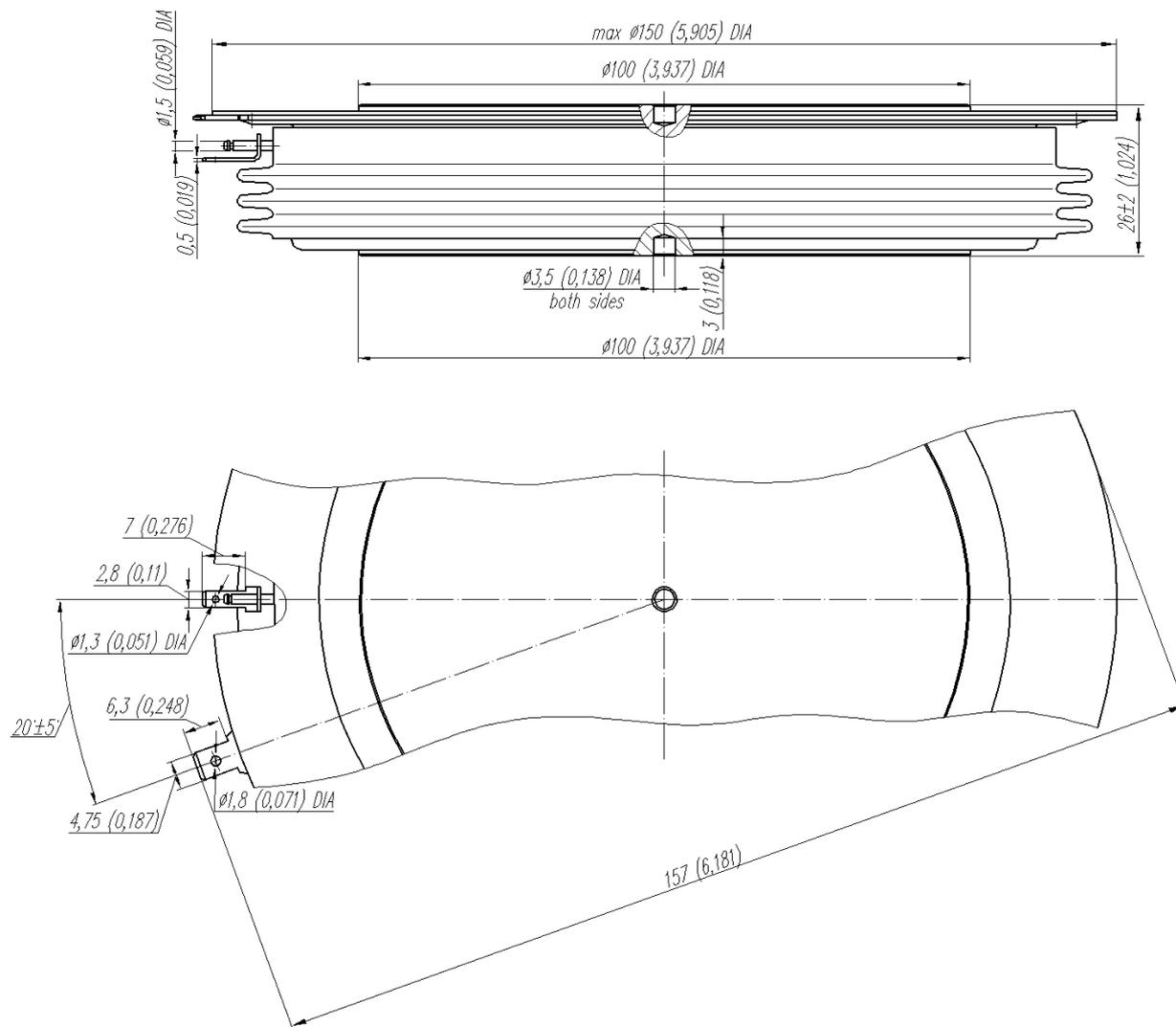
All dimensions in millimeters (inches)