EVLYS LTD. - POWER SEMICONDUCTORS DEVICES - Wholesale and Retail.

Phase Control Disc Thyristor Type DT40-800-18

High power cycling capability / Low on-state and switching losses
Designed for traction and industrial applications

Mean on-state current			I_{TAV}		800 A		
Repetitive peak off-state voltage			V_{DRM}		1000 ÷ 1800 V		
Repetitive peak reverse voltage			V_{RRM}				
Turn-off time			t_q		160, 200, 250, 320, 400, 500 µs		
V_{DRM}, V_{RRM}, V	1000	1100	1200	1300	1400	1500	1600	1800
Voltage code	10	11	12	13	14	15	16	18
T_j, °C	-60 ÷ 125							

MAXIMUM ALLOWABLE RATINGS

Symbols and parameters		Units	Values	Test conditions
ON-STATE				
I_{TAV}	Mean on-state current	A	800 770	T_c=82 °C, Double side cooled T_c=85 °C, Double side cooled 180° half-sine wave; 50 Hz
I_{TRMS}	RMS on-state current	A	1256	T_c=82 °C, Double side cooled 180° half-sine wave; 50 Hz
I_{TSM}	Surge on-state current	kA	16.0 18.0	T_j=$T_{j\,max}$ T_j=25 °C : 180° half-sine wave; 50 Hz (t_p=10 ms); single pulse; V_D=V_R=0 V; Gate pulse: I_G=2 A; t_{GP}=50 µs; di_G/dt≥1 A/µs
			17.0 20.0	T_j=$T_{j\,max}$ T_j=25 °C : 180° half-sine wave; 60 Hz (t_p=8.3 ms); single pulse; V_D=V_R=0 V; Gate pulse: I_G=2 A; t_{GP}=50 µs; di_G/dt≥1 A/µs
I^2t	Safety factor	A²s·10³	1280 1620	T_j=$T_{j\,max}$ T_j=25 °C : 180° half-sine wave; 50 Hz (t_p=10 ms); single pulse; V_D=V_R=0 V; Gate pulse: I_G=2 A; t_{GP}=50 µs; di_G/dt≥1 A/µs
			1195 1660	T_j=$T_{j\,max}$ T_j=25 °C : 180° half-sine wave; 60 Hz (t_p=8.3 ms); single pulse; V_D=V_R=0 V; Gate pulse: I_G=2 A; t_{GP}=50 µs; di_G/dt≥1 A/µs
BLOCKING				
V_{DRM}, V_{RRM}	Repetitive peak off-state and Repetitive peak reverse voltages	V	1000÷1800	$T_{j\,min}$< T_j <$T_{j\,max}$; 180° half-sine wave; 50 Hz; Gate open
V_{DSM}, V_{RSM}	Non-repetitive peak off-state and Non-repetitive peak reverse voltages	V	1100÷1900	$T_{j\,min}$< T_j <$T_{j\,max}$; 180° half-sine wave; 50 Hz;single pulse; Gate open
V_D, V_R	Direct off-state and Direct reverse voltages	V	0.75·V_{DRM} 0.75·V_{RRM}	T_j=$T_{j\,max}$; Gate open

TRIGGERING				
I_{FGM}	Peak forward gate current	A	8	$T_j=T_{j\,max}$
V_{RGM}	Peak reverse gate voltage	V	5	
P_G	Gate power dissipation	W	4	$T_j=T_{j\,max}$ for DC gate current
SWITCHING				
$(di_T/dt)_{crit}$	Critical rate of rise of on-state current non-repetitive (f=1 Hz)	A/μs	400	$T_j=T_{j\,max}$; $V_D=0.67 \cdot V_{DRM}$; $I_{TM}=2\,I_{TAV}$; Gate pulse: $I_G=2$ A; $t_{GP}=50\ \mu s$; $di_G/dt \geq 1$ A/μs
THERMAL				
T_{stg}	Storage temperature	°C	-60÷50	
T_j	Operating junction temperature	°C	-60÷125	
MECHANICAL				
F	Mounting force	kN	14.0÷16.0	
a	Acceleration	m/s^2	50 / 100	Device unclamped / Device clamped

CHARACTERISTICS

Symbols and parameters		Units	Values	Conditions	
ON-STATE					
V_{TM}	Peak on-state voltage, max	V	1.70	$T_j=25$ °C; $I_{TM}=2512$ A	
$V_{T(TO)}$	On-state threshold voltage, max	V	1.00	$T_j=T_{j\,max}$;	
r_T	On-state slope resistance, max	mΩ	0.330	$0.5\ \pi\ I_{TAV} < I_T < 1.5\ \pi\ I_{TAV}$	
I_L	Latching current, max	mA	1000	$T_j=25$ °C; $V_D=12$ V; Gate pulse: $I_G=2$ A; $t_{GP}=50\ \mu s$; $di_G/dt \geq 1$ A/μs	
I_H	Holding current, max	mA	300	$T_j=25$ °C; $V_D=12$ V; Gate open	
BLOCKING					
I_{DRM}, I_{RRM}	Repetitive peak off-state and Repetitive peak reverse currents, max	mA	100	$T_j=T_{j\,max}$; $V_D=V_{DRM}$; $V_R=V_{RRM}$	
$(dv_D/dt)_{crit}$	Critical rate of rise of off-state voltage[1], min	V/μs	200, 320, 500, 1000	$T_j=T_{j\,max}$; $V_D=0.67 \cdot V_{DRM}$; Gate open	
TRIGGERING					
V_{GT}	Gate trigger direct voltage, max	V	4.00 / 2.50 / 2.00	$T_j=T_{j\,min}$ / $T_j=25$ °C / $T_j=T_{j\,max}$	$V_D=12$ V; $I_D=3$ A; Direct gate current
I_{GT}	Gate trigger direct current, max	mA	400 / 250 / 200	$T_j=T_{j\,min}$ / $T_j=25$ °C / $T_j=T_{j\,max}$	
V_{GD}	Gate non-trigger direct voltage, min	V	0.25	$T_j=T_{j\,max}$; $V_D=0.67 \cdot V_{DRM}$; Direct gate current	
I_{GD}	Gate non-trigger direct current, min	mA	10.00		
SWITCHING					
t_{gd}	Delay time	μs	2.00	$T_j=25$ °C; $V_D=0.4 \cdot V_{DRM}$; $I_{TM}=I_{TAV}$; Gate pulse: $I_G=2$ A; $t_{GP}=50\ \mu s$; $di_G/dt \geq 1$ A/μs	
t_q	Turn-off time[2], max	μs	160, 200, 250, 320, 400, 500	$dv_D/dt=50$ V/μs; $T_j=T_{j\,max}$; $I_{TM}=I_{TAV}$; $di_R/dt=-10$ A/μs; $V_R=100$V; $V_D=0.67 \cdot V_{DRM}$	

THERMAL

R_{thjc}	Thermal resistance, junction to case, max	°C/W	0.0320	Direct current	Double side cooled
R_{thjc-A}			0.0704		Anode side cooled
R_{thjc-K}			0.0576		Cathode side cooled
R_{thck}	Thermal resistance, case to heatsink, max	°C/W	0.0060	Direct current	

MECHANICAL

w	Weight, typ	g	260	
D_s	Surface creepage distance	mm (inch)	19.44 (0.765)	
D_a	Air strike distance	mm (inch)	12.10 (0.476)	

PART NUMBERING GUIDE

DT   40   800   18   7   3

1   2   3   4   5   6

1. DT - Phase Control Disc Thyristor
2. Element Diameter
3. Mean on-state current, A
4. Voltage code
5. Critical rate of rise of on-state current non-repetitive, V/µs
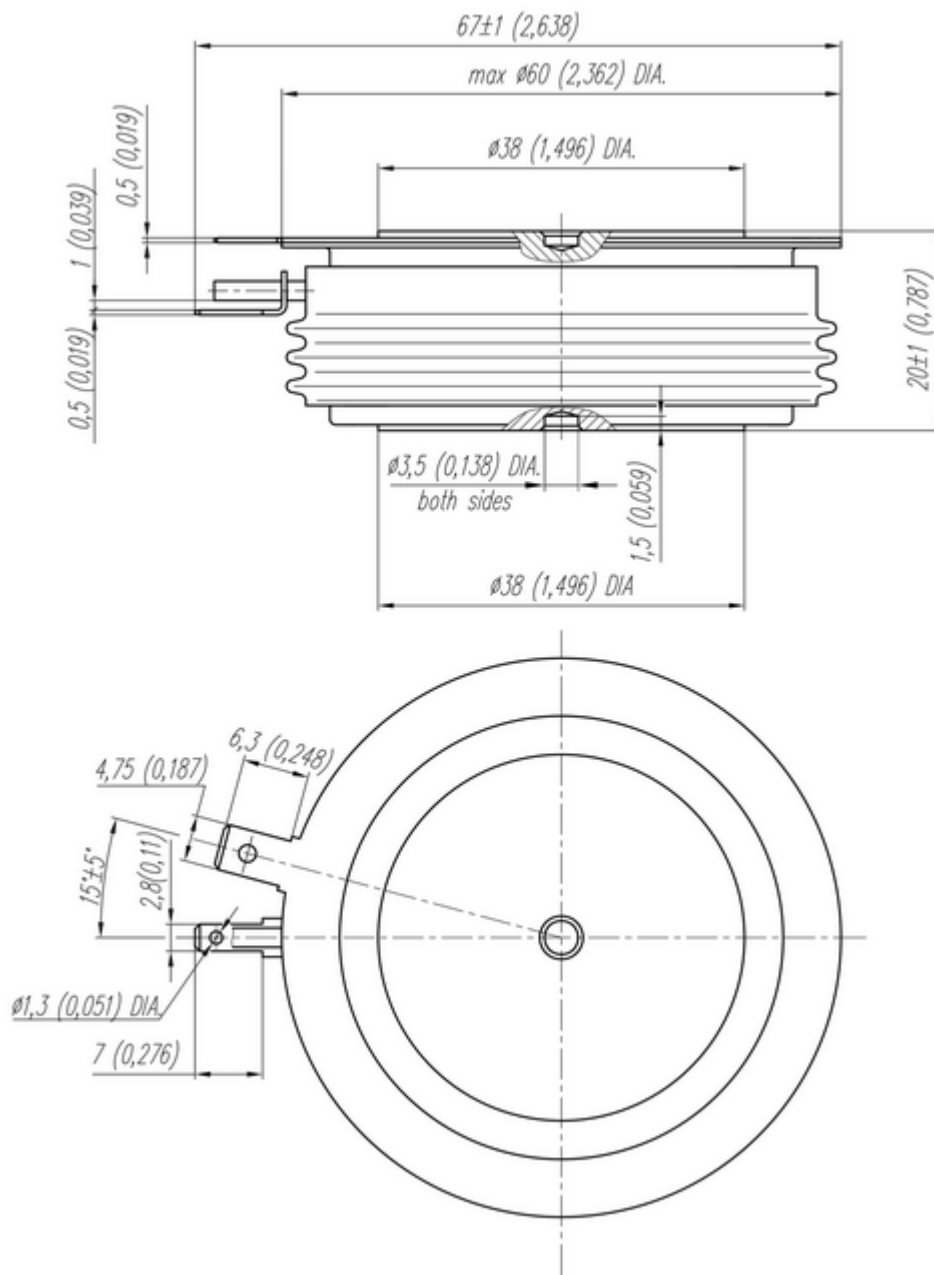6. Turn-off time (dv_D/dt=50 V/µs)

NOTES

1) Critical rate of rise of on-state current non-repetitive

Symbol of Group	4	5	6	7
$(dv_D/dt)_{crit}$, V/µs	200	320	500	1000

2) Turn-off time (dv_D/dt=50 V/µs)

Symbol of Group	3	0	0	0	0	0
t_q, µs	160	200	250	320	400	500

67±1 (2,638)

max ⌀60 (2,362) DIA.

⌀38 (1,496) DIA.

0,5 (0,019)

1 (0,039)

0,5 (0,019)

20±1 (0,787)

⌀3,5 (0,138) DIA.
both sides

1,5 (0,059)

⌀38 (1,496) DIA

6,3 (0,248)

4,75 (0,187)

15°±5°

2,8 (0,11)

⌀1,3 (0,051) DIA.

7 (0,276)

All dimensions in millimeters (inches)