

Phase Control Disc Thyristor Type DT56-500-65

High power cycling capability / Low on-state and switching losses
Designed for traction and industrial applications

Mean on-state current	I_{TAV}		500 A									
Repetitive peak off-state voltage	V_{DRM}		4600 ÷ 6500 V									
Repetitive peak reverse voltage	V_{RRM}											
Turn-off time	t_q		800 μ s									
V_{DRM}, V_{RRM}, V	4600	4800	5000	5200	5400	5600	5800	6000	6200	6400	6500	
Voltage code	46	48	50	52	54	56	58	60	62	64	65	
$T_j, ^\circ C$	-60 ÷ 125											

MAXIMUM ALLOWABLE RATINGS

Symbols and parameters		Units	Values	Test conditions
ON-STATE				
I_{TAV}	Mean on-state current	A	500 651	$T_c=98^\circ C$, Double side cooled $T_c=85^\circ C$, Double side cooled 180° half-sine wave; 50 Hz
I_{TRMS}	RMS on-state current	A	785	$T_c=98^\circ C$, Double side cooled 180° half-sine wave; 50 Hz
I_{TSM}	Surge on-state current	kA	9.5 11.0	$T_j=T_{jmax}$ $T_j=25^\circ C$ 180° half-sine wave; $t_p=10$ ms; single pulse; $V_D=V_R=0$ V; Gate pulse: $I_G=2$ A; $t_{GP}=50$ μ s; $di_G/dt \geq 1$ A/ μ s
			10.0 11.5	$T_j=T_{jmax}$ $T_j=25^\circ C$ 180° half-sine wave; $t_p=8.3$ ms; single pulse; $V_D=V_R=0$ V; Gate pulse: $I_G=2$ A; $t_{GP}=50$ μ s; $di_G/dt \geq 1$ A/ μ s
I^2t	Safety factor	$A^2s \cdot 10^3$	450 600	$T_j=T_{jmax}$ $T_j=25^\circ C$ 180° half-sine wave; $t_p=10$ ms; single pulse; $V_D=V_R=0$ V; Gate pulse: $I_G=2$ A; $t_{GP}=50$ μ s; $di_G/dt \geq 1$ A/ μ s
			410 540	$T_j=T_{jmax}$ $T_j=25^\circ C$ 180° half-sine wave; $t_p=8.3$ ms; single pulse; $V_D=V_R=0$ V; Gate pulse: $I_G=2$ A; $t_{GP}=50$ μ s; $di_G/dt \geq 1$ A/ μ s
BLOCKING				
V_{DRM}, V_{RRM}	Repetitive peak off-state and Repetitive peak reverse voltages	V	4600 ÷ 6500	$T_{jmin} < T_j < T_{jmax}$; 180° half-sine wave; 50 Hz; Gate open
V_{DSM}, V_{RSM}	Non-repetitive peak off-state and Non-repetitive peak reverse voltages	V	4700 ÷ 6600	$T_{jmin} < T_j < T_{jmax}$; 180° half-sine wave; single pulse; Gate open
V_D, V_R	Direct off-state and Direct reverse voltages	V	$0.6 \cdot V_{DRM}$ $0.6 \cdot V_{RRM}$	$T_j = T_{jmax}$; Gate open

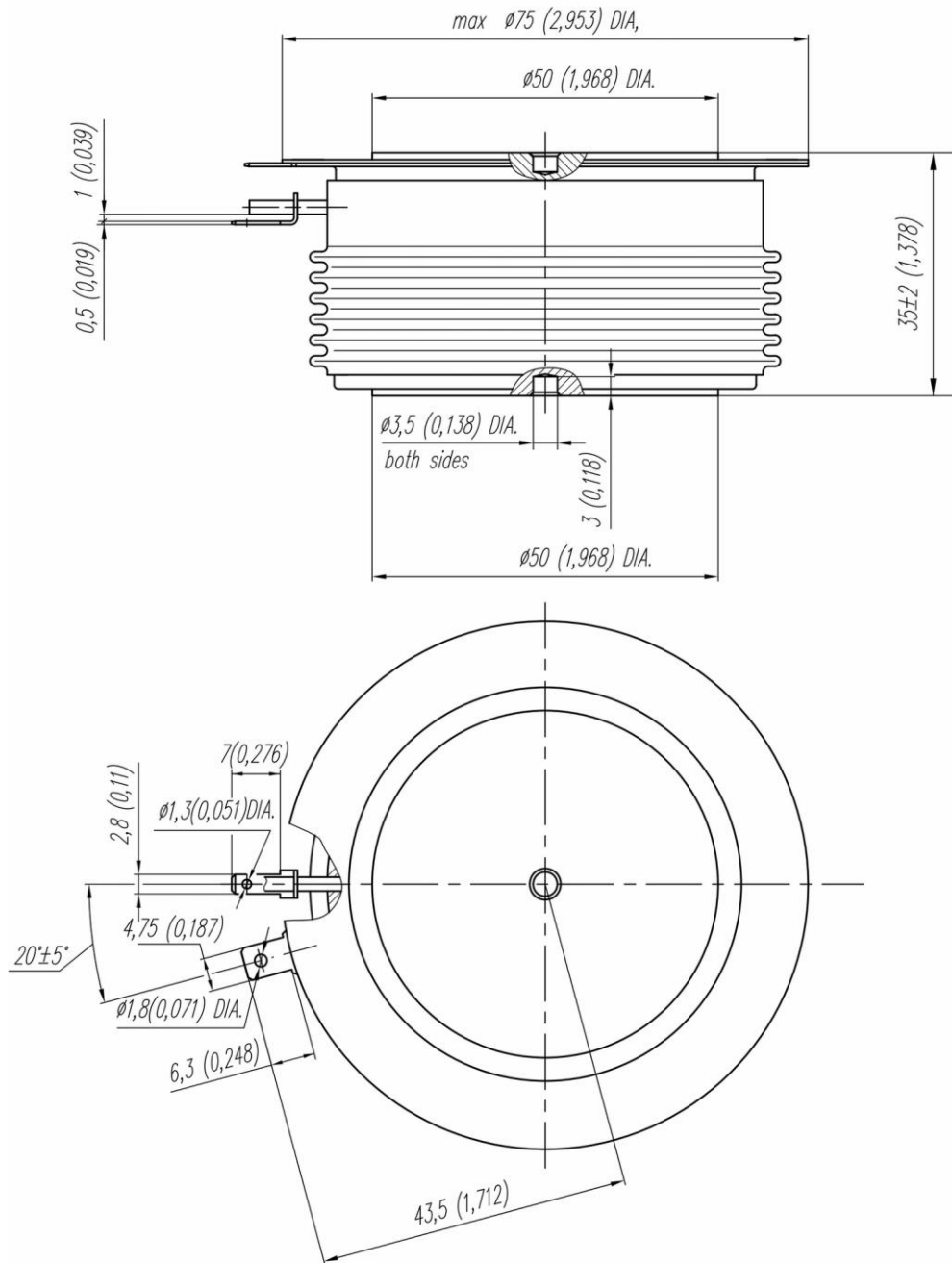
TRIGGERING				
I_{FGM}	Peak forward gate current	A	8	$T_j = T_{j \max}$
V_{RGM}	Peak reverse gate voltage	V	5	
P_G	Gate power dissipation	W	4	$T_j = T_{j \max}$ for DC gate current
SWITCHING				
$(di_T/dt)_{crit}$	Critical rate of rise of on-state current non-repetitive (f=1 Hz)	A/ μ S	400	$T_j = T_{j \max}$; $V_D = 0.67 \cdot V_{DRM}$; $I_{TM} = 2150$ A; Gate pulse: $I_G = 2$ A; $t_{GP} = 50$ μ S; $di_G/dt \geq 2$ A/ μ S
THERMAL				
T_{stg}	Storage temperature	$^{\circ}$ C	-60 ÷ 50	
T_j	Operating junction temperature	$^{\circ}$ C	-60 ÷ 125	
MECHANICAL				
F	Mounting force	kN	24.0 ÷ 28.0	
a	Acceleration	m/s ²	50	Device clamped

CHARACTERISTICS

Symbols and parameters		Units	Values	Conditions	
ON-STATE					
V_{TM}	Peak on-state voltage, max	V	2.50	$T_j = 25$ $^{\circ}$ C; $I_{TM} = 1570$ A	
$V_{T(TO)}$	On-state threshold voltage, max	V	1.272	$T_j = T_{j \max}$;	
r_T	On-state slope resistance, max	m Ω	1.125	$0.5 \pi I_{TAV} < I_T < 1.5 \pi I_{TAV}$	
I_L	Latching current, max	mA	1500	$T_j = 25$ $^{\circ}$ C; $V_D = 12$ V; Gate pulse: $I_G = 2$ A; $t_{GP} = 50$ μ S; $di_G/dt \geq 1$ A/ μ S	
I_H	Holding current, max	mA	300	$T_j = 25$ $^{\circ}$ C; $V_D = 12$ V; Gate open	
BLOCKING					
I_{DRM}, I_{RRM}	Repetitive peak off-state and Repetitive peak reverse currents, max	mA	200	$T_j = T_{j \max}$; $V_D = V_{DRM}$; $V_R = V_{RRM}$	
$(dv_D/dt)_{crit}$	Critical rate of rise of off-state voltage ¹⁾ , min	V/ μ S	1000, 1600, 2000, 2500	$T_j = T_{j \max}$; $V_D = 0.67 \cdot V_{DRM}$; Gate open	
TRIGGERING					
V_{GT}	Gate trigger direct voltage, max	V	3.00	$T_j = T_{j \min}$	$V_D = 12$ V; $I_D = 3$ A; Direct gate current
			2.50	$T_j = 25$ $^{\circ}$ C	
			1.50	$T_j = T_{j \max}$	
I_{GT}	Gate trigger direct current, max	mA	400	$T_j = T_{j \min}$	
			250	$T_j = 25$ $^{\circ}$ C	
			150	$T_j = T_{j \max}$	
V_{GD}	Gate non-trigger direct voltage, min	V	0.45	$T_j = T_{j \max}$; $V_D = 0.67 \cdot V_{DRM}$;	
I_{GD}	Gate non-trigger direct current, min	mA	65.00	Direct gate current	
SWITCHING					
t_{gd}	Delay time, max	μ S	3.00	$T_j = 25$ $^{\circ}$ C; $V_D = 1500$ V; $I_{TM} = I_{TAV}$; $di/dt = 200$ A/ μ S;	
t_{gt}	Turn-on time, max	μ S	10.00	Gate pulse: $I_G = 2$ A; $V_G = 20$ V; $t_{GP} = 50$ μ S; $di_G/dt = 2$ A/ μ S	
t_q	Turn-off time ²⁾ , max	μ S	800	$dv_D/dt = 50$ V/ μ S; $T_j = T_{j \max}$; $I_{TM} = I_{TAV}$; $di_R/dt = -10$ A/ μ S; $V_R = 100$ V; $V_D = 2000$ V	
Q_{rr}	Total recovered charge, max	μ C	4500	$T_j = T_{j \max}$; $I_{TM} = 1000$ A;	
t_{rr}	Reverse recovery time, typ	μ S	60.0	$di_R/dt = -5$ A/ μ S;	
I_{rrM}	Peak reverse recovery current, max	A	150	$V_R = 100$ V	

THERMAL					
R_{thjc}	Thermal resistance, junction to case, max	°C/W	0.020	Direct current	Double side cooled
R_{thjc-A}			0.044		Anode side cooled
R_{thjc-K}			0.036		Cathode side cooled
R_{thck}	Thermal resistance, case to heatsink, max	°C/W	0.004	Direct current	
MECHANICAL					
w	Weight, max	g	700		
D_s	Surface creepage distance	mm (inch)	39.55 (1.557)		
D_a	Air strike distance	mm (inch)	25.50 (1.004)		

PART NUMBERING GUIDE							NOTES														
DT	56	500	65	7	0		1) Critical rate of rise of off-state voltage														
1	2	3	4	5	6		<table border="1"> <thead> <tr> <th>Symbol of Group</th> <th>7</th> <th>8</th> <th>8.5</th> <th>9</th> </tr> </thead> <tbody> <tr> <td>$(dv_D/dt)_{crit}, V/\mu s$</td> <td>1000</td> <td>1600</td> <td>2000</td> <td>2500</td> </tr> </tbody> </table>					Symbol of Group	7	8	8.5	9	$(dv_D/dt)_{crit}, V/\mu s$	1000	1600	2000	2500
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1. DT - Phase Control Disc Thyristor 2. Element Diameter 3. Mean on-state current, A 4. Voltage code 5. Critical rate of rise of on-state current non-repetitive, V/ μs 6. Turn-off time ($dv_D/dt=50 V/\mu s$)							2) Turn-off time ($dv_D/dt=50 V/\mu s$)														
							<table border="1"> <thead> <tr> <th>Symbol of Group</th> <th colspan="4">0</th> </tr> </thead> <tbody> <tr> <td>$t_q, \mu s$</td> <td colspan="4">800</td> </tr> </tbody> </table>					Symbol of Group	0				$t_q, \mu s$	800			
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All dimensions in millimeters (inches)