EVLYS LTD. - POWER SEMICONDUCTORS DEVICES - Wholesale and Retail.

Phase Control Disc Thyristor Type DT40-400-44

High power cycling capability / Low on-state and switching losses
Designed for traction and industrial applications

Mean on-state current		I_{TAV}	400 A	
Repetitive peak off-state voltage		V_{DRM}	3800 ÷ 4400 V	
Repetitive peak reverse voltage		V_{RRM}		
Turn-off time		t_q	500, 630, 800 µs	
V_{DRM}, V_{RRM}, V	3800	4000	4200	4400
Voltage code	38	40	42	44
T_j, °C	-60 ÷ 125			

MAXIMUM ALLOWABLE RATINGS

Symbols and parameters		Units	Values	Test conditions	
ON-STATE					
I_{TAV}	Mean on-state current	A	400 460	T_c=92 °C, Double side cooled T_c=85 °C, Double side cooled 180° half-sine wave; 50 Hz	
I_{TRMS}	RMS on-state current	A	628	T_c=92 °C, Double side cooled 180° half-sine wave; 50 Hz	
I_{TSM}	Surge on-state current	kA	8.0 9.0	T_j=$T_{j\,max}$ T_j=25 °C	180° half-sine wave; t_p=10 ms; single pulse; V_D=V_R=0 V; Gate pulse: I_G=2 A; t_{GP}=50 µs; di_G/dt≥1 A/µs
			9.0 10.4	T_j=$T_{j\,max}$ T_j=25 °C	180° half-sine wave; t_p=8.3 ms; single pulse; V_D=V_R=0 V; Gate pulse: I_G=2 A; t_{GP}=50 µs; di_G/dt≥1 A/µs
I^2t	Safety factor	$A^2s \cdot 10^3$	320 420	T_j=$T_{j\,max}$ T_j=25 °C	180° half-sine wave; t_p=10 ms; single pulse; V_D=V_R=0 V; Gate pulse: I_G=2 A; t_{GP}=50 µs; di_G/dt≥1 A/µs
			335 445	T_j=$T_{j\,max}$ T_j=25 °C	180° half-sine wave; t_p=8.3 ms; single pulse; V_D=V_R=0 V; Gate pulse: I_G=2 A; t_{GP}=50 µs; di_G/dt≥1 A/µs
BLOCKING					
V_{DRM}, V_{RRM}	Repetitive peak off-state and Repetitive peak reverse voltages	V	3800÷4400	$T_{j\,min}$< T_j <$T_{j\,max}$; 180° half-sine wave; 50 Hz; Gate open	
V_{DSM}, V_{RSM}	Non-repetitive peak off-state and Non-repetitive peak reverse voltages	V	3900÷4500	$T_{j\,min}$< T_j <$T_{j\,max}$; 180° half-sine wave; single pulse; Gate open	
V_D, V_R	Direct off-state and Direct reverse voltages	V	0.75·V_{DRM} 0.75·V_{RRM}	T_j=$T_{j\,max}$; Gate open	

TRIGGERING				
I_{FGM}	Peak forward gate current	A	8	$T_j=T_{j\,max}$
V_{RGM}	Peak reverse gate voltage	V	5	
P_G	Gate power dissipation	W	4	$T_j=T_{j\,max}$ for DC gate current
SWITCHING				
$(di_T/dt)_{crit}$	Critical rate of rise of on-state current non-repetitive (f=1 Hz)	A/μs	400	$T_j=T_{j\,max}$; $V_D=0.67\cdot V_{DRM}$; $I_{TM}=2\ I_{TAV}$; Gate pulse: $I_G=2$ A; $t_{GP}=50$ μs; $di_G/dt\geq 2$ A/μs
THERMAL				
T_{stg}	Storage temperature	°C	-60÷50	
T_j	Operating junction temperature	°C	-60÷125	
MECHANICAL				
F	Mounting force	kN	14.0÷16.0	
a	Acceleration	m/s^2	50 100	Device unclamped Device clamped

CHARACTERISTICS

Symbols and parameters		Units	Values	Conditions	
ON-STATE					
V_{TM}	Peak on-state voltage, max	V	2.35	$T_j=25$ °C; $I_{TM}=1256$ A	
$V_{T(TO)}$	On-state threshold voltage, max	V	1.30	$T_j=T_{j\,max}$; $0.5\ \pi\ I_{TAV} < I_T < 1.5\ \pi\ I_{TAV}$	
r_T	On-state slope resistance, max	mΩ	1.250		
I_L	Latching current, max	mA	1000	$T_j=25$ °C; $V_D=12$ V; Gate pulse: $I_G=2$ A; $t_{GP}=50$ μs; $di_G/dt\geq 1$ A/μs	
I_H	Holding current, max	mA	300	$T_j=25$ °C; $V_D=12$ V; Gate open	
BLOCKING					
I_{DRM}, I_{RRM}	Repetitive peak off-state and Repetitive peak reverse currents, max	mA	100	$T_j=T_{j\,max}$; $V_D=V_{DRM}$; $V_R=V_{RRM}$	
$(dv_D/dt)_{crit}$	Critical rate of rise of off-state voltage[1)], min	V/μs	200, 320, 500, 1000	$T_j=T_{j\,max}$; $V_D=0.67\cdot V_{DRM}$; Gate open	
TRIGGERING					
V_{GT}	Gate trigger direct voltage, max	V	5.00 3.00 2.00	$T_j=T_{j\,min}$ $T_j=25$ °C $T_j=T_{j\,max}$	$V_D=12$ V; $I_D=3$ A; Direct gate current
I_{GT}	Gate trigger direct current, max	mA	500 300 200	$T_j=T_{j\,min}$ $T_j=25$ °C $T_j=T_{j\,max}$	
V_{GD}	Gate non-trigger direct voltage, min	V	0.25	$T_j=T_{j\,max}$; $V_D=0.67\cdot V_{DRM}$; Direct gate current	
I_{GD}	Gate non-trigger direct current, min	mA	10.00		
SWITCHING					
t_{gd}	Delay time	μs	3.50	$T_j=25$ °C; $V_D=0.4\cdot V_{DRM}$; $I_{TM}=I_{TAV}$; Gate pulse: $I_G=2$ A; $t_{GP}=50$ μs; $di_G/dt\geq 2$ A/μs	
t_q	Turn-off time[2)], max	μs	500, 630, 800	$dv_D/dt=50$ V/μs; $T_j=T_{j\,max}$; $I_{TM}=I_{TAV}$; $di_R/dt=-10$ A/μs; $V_R=100$V; $V_D=0.67\cdot V_{DRM}$	
Q_{rr}	Total recovered charge, max	μC	2000	$T_j=T_{j\,max}$; $I_{TM}=400$ A; $di_R/dt=-5$ A/μs; $V_R=100$ V	
t_{rr}	Reverse recovery time, max	μs	50		
I_{rrM}	Peak reverse recovery current, max	A	80		

R_{thjc}	Thermal resistance, junction to case, max	°C/W	0.0320	Direct current	Double side cooled
R_{thjc-A}			0.0704		Anode side cooled
R_{thjc-K}			0.0576		Cathode side cooled
R_{thck}	Thermal resistance, case to heatsink, max	°C/W	0.0060	Direct current	
MECHANICAL					
w	Weight, typ	g	260		
D_s	Surface creepage distance	mm (inch)	19.44 (0.765)		
D_a	Air strike distance	mm (inch)	12.10 (0.476)		

PART NUMBERING GUIDE

DT	40	400	44	7	6
1	2	3	4	5	6

1. DT - Phase Control Disc Thyristor
2. Element Diameter
3. Mean on-state current, A
4. Voltage code
5. Critical rate of rise of on-state current non-repetitive, V/µs
6. Turn-off time (dv_D/dt=50 V/µs)

NOTES

1) Critical rate of rise of off-state voltage

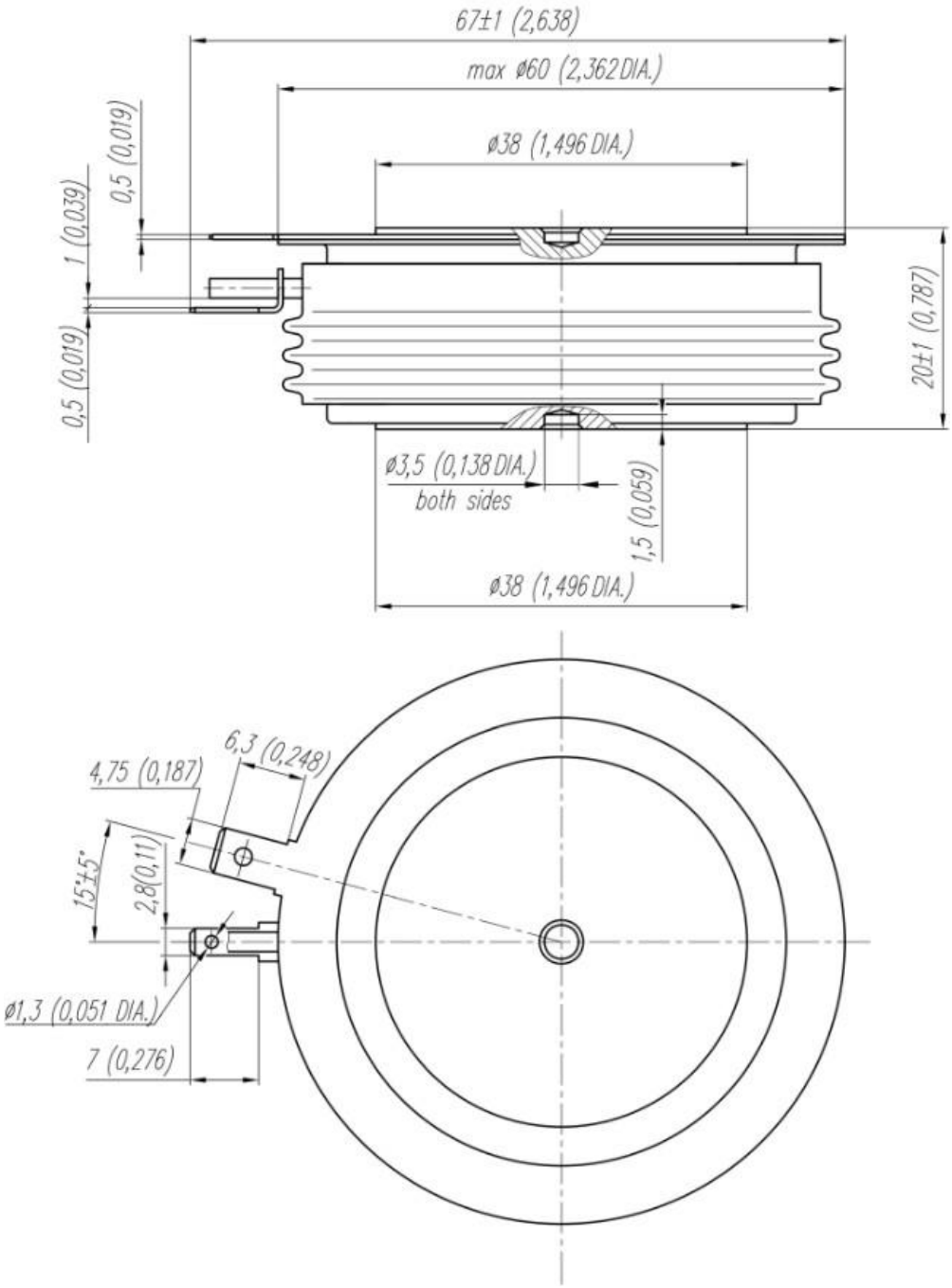
Symbol of Group	4	5	6	7
$(dv_D/dt)_{crit}$, V/µs	200	320	500	1000

2) Turn-off time (dv_D/dt=50 V/µs)

Symbol of Group	0	0	0
t_q, µs	500	630	800

OVERALL DIMENSIONS

Package type: T.C2



All dimensions in millimeters (inches)