

# EVLYS LTD. - POWER SEMICONDUCTORS DEVICES - Wholesale and Retail.

## Phase Control Disc Thyristor Type DT32-250-24

High power cycling capability / Low on-state and switching losses  
Designed for traction and industrial applications

Mean on-state current	$I_{TAV}$	250 A	
Repetitive peak off-state voltage	$V_{DRM}$	2000 ÷ 2400 V	
Repetitive peak reverse voltage	$V_{RRM}$		
Turn-off time	$t_q$	200, 250, 320, 400, 500 $\mu$ s	
$V_{DRM}, V_{RRM}, V$	2000	2200	2400
Voltage code	20	22	24
$T_j, ^\circ C$	-60 ÷ 125		

### MAXIMUM ALLOWABLE RATINGS

Symbols and parameters		Units	Values	Test conditions
<b>ON-STATE</b>				
$I_{TAV}$	Mean on-state current	A	250 480	$T_c=109^\circ C$ , Double side cooled $T_c=85^\circ C$ , Double side cooled 180° half-sine wave; 50 Hz
$I_{TRMS}$	RMS on-state current	A	392	$T_c=109^\circ C$ , Double side cooled 180° half-sine wave; 50 Hz
$I_{TSM}$	Surge on-state current	kA	8.0 9.0	$T_j=T_{jmax}$ $T_j=25^\circ C$ 180° half-sine wave; $t_p=10$ ms; single pulse; $V_D=V_R=0$ V; Gate pulse: $I_G=2$ A; $t_{GP}=50$ $\mu$ s; $di_G/dt \geq 1$ A/ $\mu$ s
			8.5 10.0	$T_j=T_{jmax}$ $T_j=25^\circ C$ 180° half-sine wave; $t_p=8.3$ ms; single pulse; $V_D=V_R=0$ V; Gate pulse: $I_G=2$ A; $t_{GP}=50$ $\mu$ s; $di_G/dt \geq 1$ A/ $\mu$ s
$I^2t$	Safety factor	$A^2s \cdot 10^3$	320 400	$T_j=T_{jmax}$ $T_j=25^\circ C$ 180° half-sine wave; $t_p=10$ ms; single pulse; $V_D=V_R=0$ V; Gate pulse: $I_G=2$ A; $t_{GP}=50$ $\mu$ s; $di_G/dt \geq 1$ A/ $\mu$ s
			290 410	$T_j=T_{jmax}$ $T_j=25^\circ C$ 180° half-sine wave; $t_p=8.3$ ms; single pulse; $V_D=V_R=0$ V; Gate pulse: $I_G=2$ A; $t_{GP}=50$ $\mu$ s; $di_G/dt \geq 1$ A/ $\mu$ s
<b>BLOCKING</b>				
$V_{DRM}, V_{RRM}$	Repetitive peak off-state and Repetitive peak reverse voltages	V	2000 ÷ 2400	$T_{jmin} < T_j < T_{jmax}$ ; 180° half-sine wave; 50 Hz; Gate open
$V_{DSM}, V_{RSM}$	Non-repetitive peak off-state and Non-repetitive peak reverse voltages	V	2100 ÷ 2500	$T_{jmin} < T_j < T_{jmax}$ ; 180° half-sine wave; single pulse; Gate open
$V_D, V_R$	Direct off-state and Direct reverse voltages	V	$0.6 \cdot V_{DRM}$ $0.6 \cdot V_{RRM}$	$T_j=T_{jmax}$ ; Gate open

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TRIGGERING				
$I_{FGM}$	Peak forward gate current	A	6	$T_j = T_{j\max}$
$V_{RGM}$	Peak reverse gate voltage	V	5	
$P_G$	Gate power dissipation	W	3	$T_j = T_{j\max}$ for DC gate current
SWITCHING				
$(di_T/dt)_{crit}$	Critical rate of rise of on-state current non-repetitive (f=1 Hz)	A/ $\mu$ s	800	$T_j = T_{j\max}$ ; $V_D = 0.67 \cdot V_{DRM}$ ; $I_{TM} = 1760$ A; Gate pulse: $I_G = 2$ A; $t_{GP} = 50$ $\mu$ s; $di_G/dt \geq 2$ A/ $\mu$ s
THERMAL				
$T_{stg}$	Storage temperature	$^{\circ}$ C	-60÷50	
$T_j$	Operating junction temperature	$^{\circ}$ C	-60÷125	
MECHANICAL				
F	Mounting force	kN	9.0÷11.0	
a	Acceleration	m/s <sup>2</sup>	50	Device clamped

## CHARACTERISTICS

Symbols and parameters		Units	Values	Conditions	
ON-STATE					
$V_{TM}$	Peak on-state voltage, max	V	1.70	$T_j = 25$ $^{\circ}$ C; $I_{TM} = 785$ A	
$V_{T(TO)}$	On-state threshold voltage, max	V	1.034	$T_j = T_{j\max}$ ;	
$r_T$	On-state slope resistance, max	m $\Omega$	0.889	$0.5 \pi I_{TAV} < I_T < 1.5 \pi I_{TAV}$	
$I_L$	Latching current, max	mA	700	$T_j = 25$ $^{\circ}$ C; $V_D = 12$ V; Gate pulse: $I_G = 2$ A; $t_{GP} = 50$ $\mu$ s; $di_G/dt \geq 1$ A/ $\mu$ s	
$I_H$	Holding current, max	mA	300	$T_j = 25$ $^{\circ}$ C; $V_D = 12$ V; Gate open	
BLOCKING					
$I_{DRM}$ , $I_{RRM}$	Repetitive peak off-state and Repetitive peak reverse currents, max	mA	70	$T_j = T_{j\max}$ ; $V_D = V_{DRM}$ ; $V_R = V_{RRM}$	
$(dv_D/dt)_{crit}$	Critical rate of rise of off-state voltage <sup>1)</sup> , min	V/ $\mu$ s	200, 320, 500, 1000, 1600, 2000, 2500	$T_j = T_{j\max}$ ; $V_D = 0.67 \cdot V_{DRM}$ ; Gate open	
TRIGGERING					
$V_{GT}$	Gate trigger direct voltage, max	V	3.00 2.50 1.50	$T_j = T_{j\min}$ $T_j = 25$ $^{\circ}$ C $T_j = T_{j\max}$	$V_D = 12$ V; $I_D = 3$ A; Direct gate current
$I_{GT}$	Gate trigger direct current, max	mA	400 250 150	$T_j = T_{j\min}$ $T_j = 25$ $^{\circ}$ C $T_j = T_{j\max}$	
$V_{GD}$	Gate non-trigger direct voltage, min	V	0.55	$T_j = T_{j\max}$ ;	
$I_{GD}$	Gate non-trigger direct current, min	mA	30.00	$V_D = 0.67 \cdot V_{DRM}$ ; Direct gate current	
SWITCHING					
$t_{gd}$	Delay time, max	$\mu$ s	1.10	$T_j = 25$ $^{\circ}$ C; $V_D = 1000$ V; $I_{TM} = I_{TAV}$ ; $di/dt = 200$ A/ $\mu$ s;	
$t_{gt}$	Turn-on time, max	$\mu$ s	8.00	Gate pulse: $I_G = 2$ A; $V_G = 20$ V; $t_{GP} = 50$ $\mu$ s; $di_G/dt = 2$ A/ $\mu$ s	
$t_q$	Turn-off time <sup>2)</sup> , max	$\mu$ s	200, 250, 320, 400, 500	$dv_D/dt = 50$ V/ $\mu$ s; $T_j = T_{j\max}$ ; $I_{TM} = I_{TAV}$ ; $di_R/dt = -10$ A/ $\mu$ s; $V_R = 100$ V; $V_D = 0.67 \cdot V_{DRM}$	
$Q_{rr}$	Total recovered charge, max	$\mu$ C	1000	$T_j = T_{j\max}$ ; $I_{TM} = 250$ A;	
$t_{rr}$	Reverse recovery time, max	$\mu$ s	20	$di_R/dt = -10$ A/ $\mu$ s;	
$I_{rrM}$	Peak reverse recovery current, max	A	100	$V_R = 100$ V	

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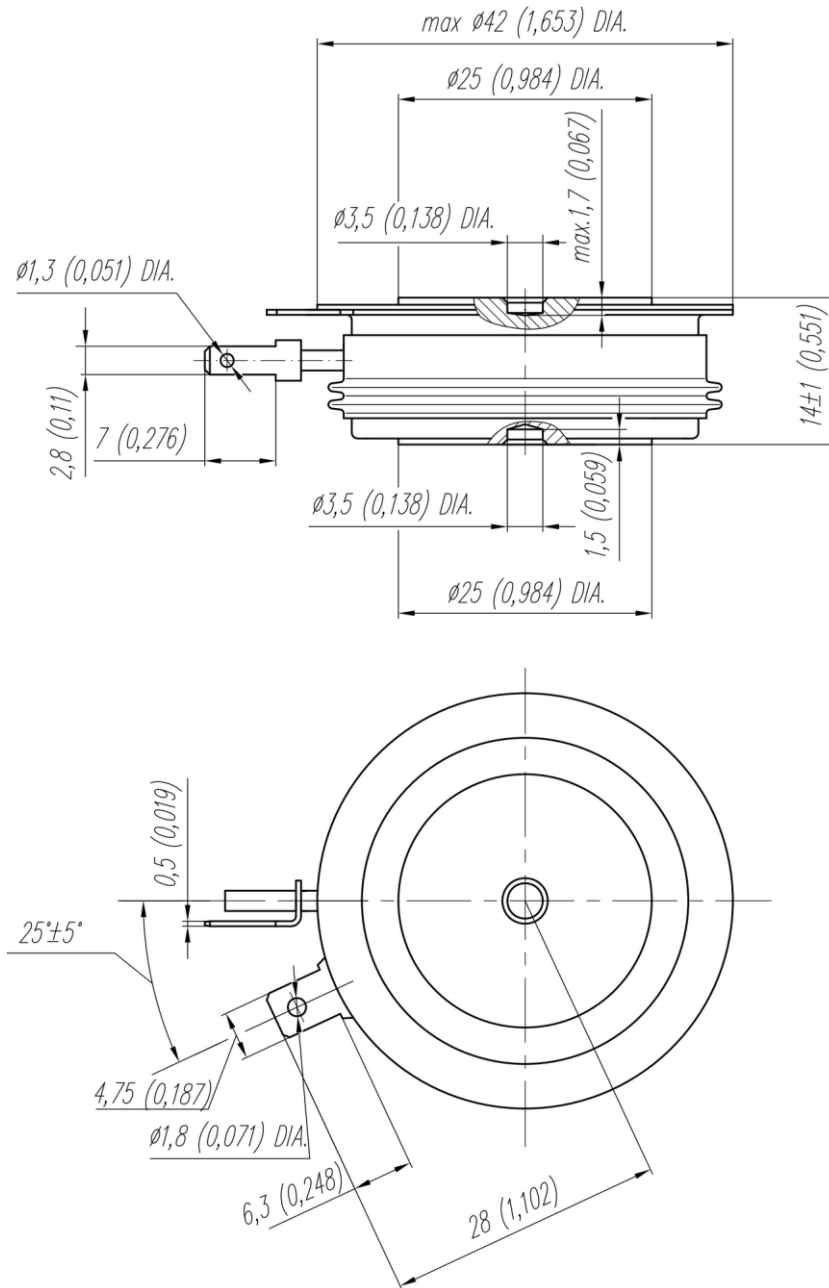
<b>THERMAL</b>					
$R_{thjc}$	Thermal resistance, junction to case, max	°C/W	0.040	Direct current	Double side cooled
$R_{thjc-A}$			0.088		Anode side cooled
$R_{thjc-K}$			0.072		Cathode side cooled
$R_{thck}$	Thermal resistance, case to heatsink, max	°C/W	0.008	Direct current	
<b>MECHANICAL</b>					
w	Weight, max	g	110		
$D_s$	Surface creepage distance	mm (inch)	10.30 (0.405)		
$D_a$	Air strike distance	mm (inch)	6.30 (0.248)		

<b>PART NUMBERING GUIDE</b>							<b>NOTES</b>																						
DT	32	250	24	7	5		1) Critical rate of rise of off-state voltage																						
1	2	3	4	5	6		<table border="1" style="width: 100%;"> <thead> <tr> <th>Symbol of Group</th> <th>4</th> <th>5</th> <th>6</th> <th>7</th> <th>8</th> <th>8.5</th> <th>9</th> </tr> </thead> <tbody> <tr> <td><math>(dv_b/dt)_{crit}</math>, V/<math>\mu</math>s</td> <td>200</td> <td>320</td> <td>500</td> <td>1000</td> <td>1600</td> <td>2000</td> <td>2500</td> </tr> </tbody> </table>							Symbol of Group	4	5	6	7	8	8.5	9	$(dv_b/dt)_{crit}$ , V/ $\mu$ s	200	320	500	1000	1600	2000	2500
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## OVERALL DIMENSIONS

Package type: T.B2



All dimensions in millimeters (inches)