

EVLYS LTD. - POWER SEMICONDUCTORS DEVICES - Wholesale and Retail.

Phase Control Disc Thyristor Type DT24-160-36

High power cycling capability / Low on-state and switching losses
Designed for traction and industrial applications

Mean on-state current	I_{TAV}	160 A		
Repetitive peak off-state voltage	V_{DRM}	3000...3600 V		
Repetitive peak reverse voltage	V_{RRM}			
Turn-off time	t_q	400, 500 μ s		
V_{DRM}, V_{RRM}, V	3000	3200	3400	3600
Voltage code	30	32	34	36
$T_j, ^\circ C$	-60...+125			

MAXIMUM ALLOWABLE RATINGS

Symbols and parameters		Units	Values	Test conditions
ON-STATE				
I_{TAV}	Maximum allowable mean on-state current	A	160 200	$T_c=97^\circ C$, Double side cooled $T_c=85^\circ C$, Double side cooled 180° half-sine wave; 50 Hz
I_{TRMS}	RMS on-state current	A	251	$T_c=97^\circ C$, Double side cooled 180° half-sine wave; 50 Hz
I_{TSM}	Surge on-state current	kA	3.2 3.5	$T_j=T_{jmax}$ $T_j=25^\circ C$ 180° half-sine wave; $t_p=10$ ms; single pulse; $V_D=V_R=0$ V; Gate pulse: $I_G=2$ A; $t_{GP}=50$ μ s; $di_G/dt \geq 1$ A/ μ s
			3.5 4.0	$T_j=T_{jmax}$ $T_j=25^\circ C$ 180° half-sine wave; $t_p=8.3$ ms; single pulse; $V_D=V_R=0$ V; Gate pulse: $I_G=2$ A; $t_{GP}=50$ μ s; $di_G/dt \geq 1$ A/ μ s
I^2t	Safety factor	$A^2s \cdot 10^3$	50 60	$T_j=T_{jmax}$ $T_j=25^\circ C$ 180° half-sine wave; $t_p=10$ ms; single pulse; $V_D=V_R=0$ V; Gate pulse: $I_G=2$ A; $t_{GP}=50$ μ s; $di_G/dt \geq 1$ A/ μ s
			50 60	$T_j=T_{jmax}$ $T_j=25^\circ C$ 180° half-sine wave; $t_p=8.3$ ms; single pulse; $V_D=V_R=0$ V; Gate pulse: $I_G=2$ A; $t_{GP}=50$ μ s; $di_G/dt \geq 1$ A/ μ s
BLOCKING				
V_{DRM}, V_{RRM}	Repetitive peak off-state and Repetitive peak reverse voltages	V	3000...3600	$T_{jmin} < T_j < T_{jmax}$; 180° half-sine wave; 50 Hz; Gate open
V_{DSM}, V_{RSM}	Non-repetitive peak off-state and Non-repetitive peak reverse voltages	V	3100...3700	$T_{jmin} < T_j < T_{jmax}$; 180° half-sine wave; single pulse; Gate open
V_D, V_R	Direct off-state and Direct reverse voltages	V	$0.6 \cdot V_{DRM}$ $0.6 \cdot V_{RRM}$	$T_j=T_{jmax}$; Gate open

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TRIGGERING				
I_{FGM}	Peak forward gate current	A	5	$T_j = T_{j\max}$
V_{RGM}	Peak reverse gate voltage	V	5	
P_G	Gate power dissipation	W	3	$T_j = T_{j\max}$ for DC gate current
SWITCHING				
$(di_T/dt)_{crit}$	Critical rate of rise of on-state current non-repetitive ($f=1$ Hz)	A/ μ s	250	$T_j = T_{j\max}$; $V_D = 0.67 \cdot V_{DRM}$; $I_{TM} = 2 I_{TAV}$; Gate pulse: $I_G = 2$ A; $t_{GP} = 50$ μ s; $di_G/dt \geq 2$ A/ μ s
THERMAL				
T_{stg}	Storage temperature	$^{\circ}$ C	-60...+50	
T_j	Operating junction temperature	$^{\circ}$ C	-60...+125	
MECHANICAL				
F	Mounting force	kN	5.0...7.0	
a	Acceleration	m/s^2	50 100	Device unclamped Device clamped

CHARACTERISTICS

Symbols and parameters		Units	Values	Conditions	
ON-STATE					
V_{TM}	Peak on-state voltage, max	V	2.30	$T_j = 25$ $^{\circ}$ C; $I_{TM} = 503$ A	
$V_{T(TO)}$	On-state threshold voltage, max	V	0.95	$T_j = T_{j\max}$;	
r_T	On-state slope resistance, max	m Ω	3.000	$0.5 \pi I_{TAV} < I_T < 1.5 \pi I_{TAV}$	
I_L	Latching current, max	mA	500	$T_j = 25$ $^{\circ}$ C; $V_D = 12$ V; Gate pulse: $I_G = 2$ A; $t_{GP} = 50$ μ s; $di_G/dt \geq 1$ A/ μ s	
I_H	Holding current, max	mA	250	$T_j = 25$ $^{\circ}$ C; $V_D = 12$ V; Gate open	
BLOCKING					
I_{DRM} , I_{RRM}	Repetitive peak off-state and Repetitive peak reverse currents, max	mA	70	$T_j = T_{j\max}$; $V_D = V_{DRM}$; $V_R = V_{RRM}$	
$(dv_D/dt)_{crit}$	Critical rate of rise of off-state voltage ¹⁾	V/ μ s	200, 320, 500, 1000	$T_j = T_{j\max}$; $V_D = 0.67 \cdot V_{DRM}$; Gate open	
TRIGGERING					
V_{GT}	Gate trigger direct voltage, max	V	4.00	$T_j = T_{j\min}$	$V_D = 12$ V; $I_D = 3$ A; Direct gate current
			2.50	$T_j = 25$ $^{\circ}$ C	
			2.00	$T_j = T_{j\max}$	
I_{GT}	Gate trigger direct current, max	mA	500	$T_j = T_{j\min}$	
			300	$T_j = 25$ $^{\circ}$ C	
			200	$T_j = T_{j\max}$	
V_{GD}	Gate non-trigger direct voltage, min	V	0.25	$T_j = T_{j\max}$; $V_D = 0.67 \cdot V_{DRM}$;	
I_{GD}	Gate non-trigger direct current, min	mA	10.00	Direct gate current	
SWITCHING					
t_{gd}	Delay time, max	μ s	3.00	$T_j = 25$ $^{\circ}$ C; $V_D = 1500$ V; $I_{TM} = I_{TAV}$; $di/dt = 200$ A/ μ s; Gate pulse: $I_G = 2$ A; $t_{GP} = 50$ μ s; $di_G/dt \geq 2$ A/ μ s	
t_q	Turn-off time ²⁾ , max	μ s	400, 500	$dv_D/dt = 50$ V/ μ s; $T_j = T_{j\max}$; $I_{TM} = I_{TAV}$; $di_R/dt = -10$ A/ μ s; $V_R = 100$ V; $V_D = 0.67 \cdot V_{DRM}$	
Q_{rr}	Recovered charge, max	μ C	920	$T_j = T_{j\max}$; $I_{TM} = 115$ A;	
t_{rr}	Reverse recovery time, max	μ s	31	$di_R/dt = -5$ A/ μ s;	
I_{rr}	Reverse recovery current, max	A	59	$V_R = 100$ V	

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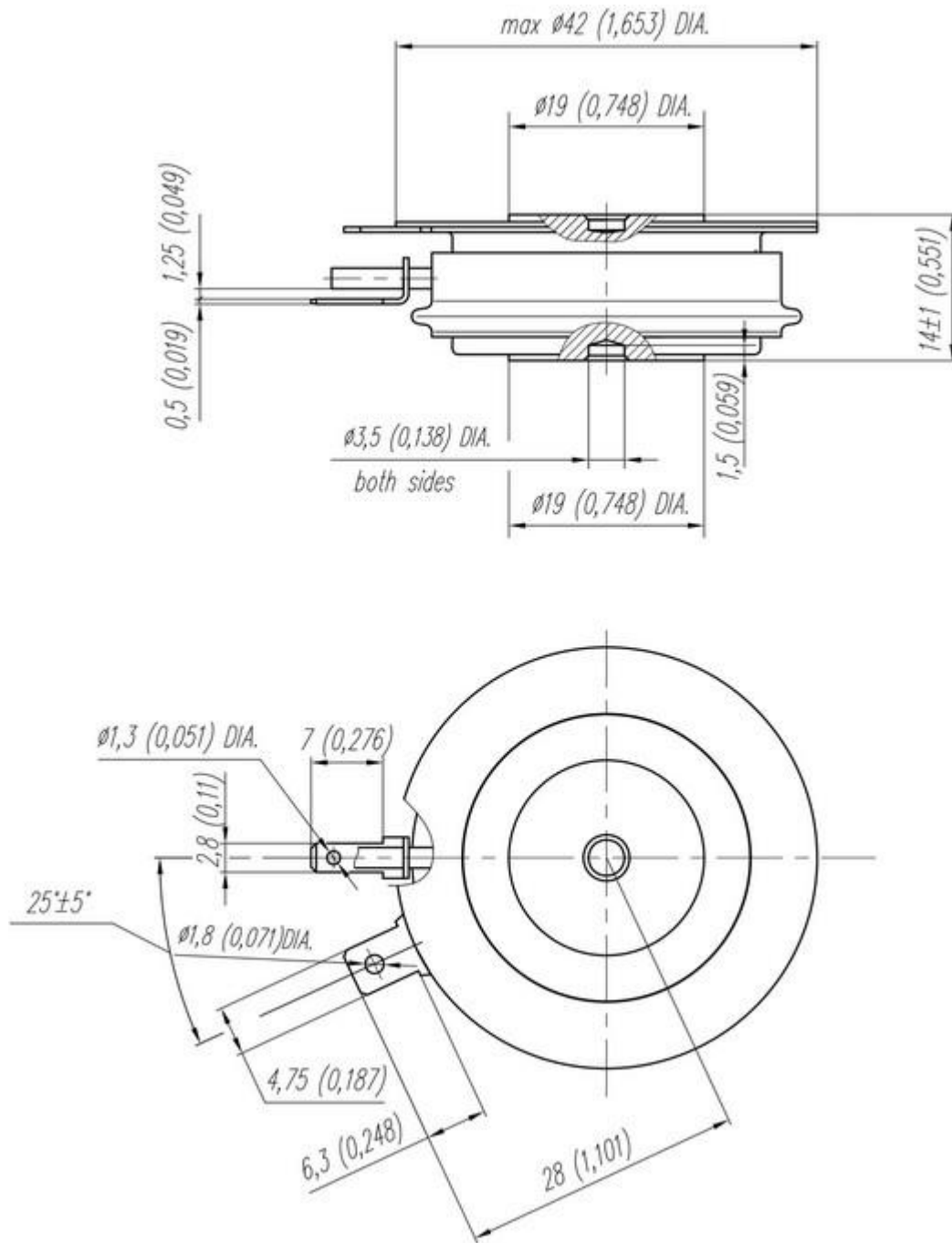
THERMAL					
R_{thjc}	Thermal resistance, junction to case, max	°C/W	0.0800	Direct current	Double side cooled
R_{thjc-A}			0.1760		Anode side cooled
R_{thjc-K}			0.1440		Cathode side cooled
R_{thck}	Thermal resistance, case to heatsink, max	°C/W	0.0100	Direct current	
MECHANICAL					
m	Weight, max	g	70		
D_s	Surface creepage distance	mm (inch)	7.94 (0.313)		
D_a	Air strike distance	mm (inch)	5.00 (0.197)		

PART NUMBERING GUIDE							NOTES					
DT	24	160	36	7	3		1) Critical rate of rise of off-state voltage					
1	2	3	4	5	6		Symbol of Group	4	5	6	7	
							$(dv_D/dt)_{crit}, V/\mu s$	200	320	500	1000	
1. DT - Phase Control Disc Thyristor							2) Turn-off time ($dv_D/dt=50 V/\mu s$)					
2. Element Diameter												
3. Mean on-state current, A												
4. Voltage code												
5. Critical rate of rise of on-state current non-repetitive, V/ μs							Symbol of group	4.5	5			
6. Turn-off time ($dv_D/dt=50 V/\mu s$)							$t_q, \mu s$	400	500			

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OVERALL DIMENSIONS

Package type: **T.A1**



All dimensions in millimeters (inches)